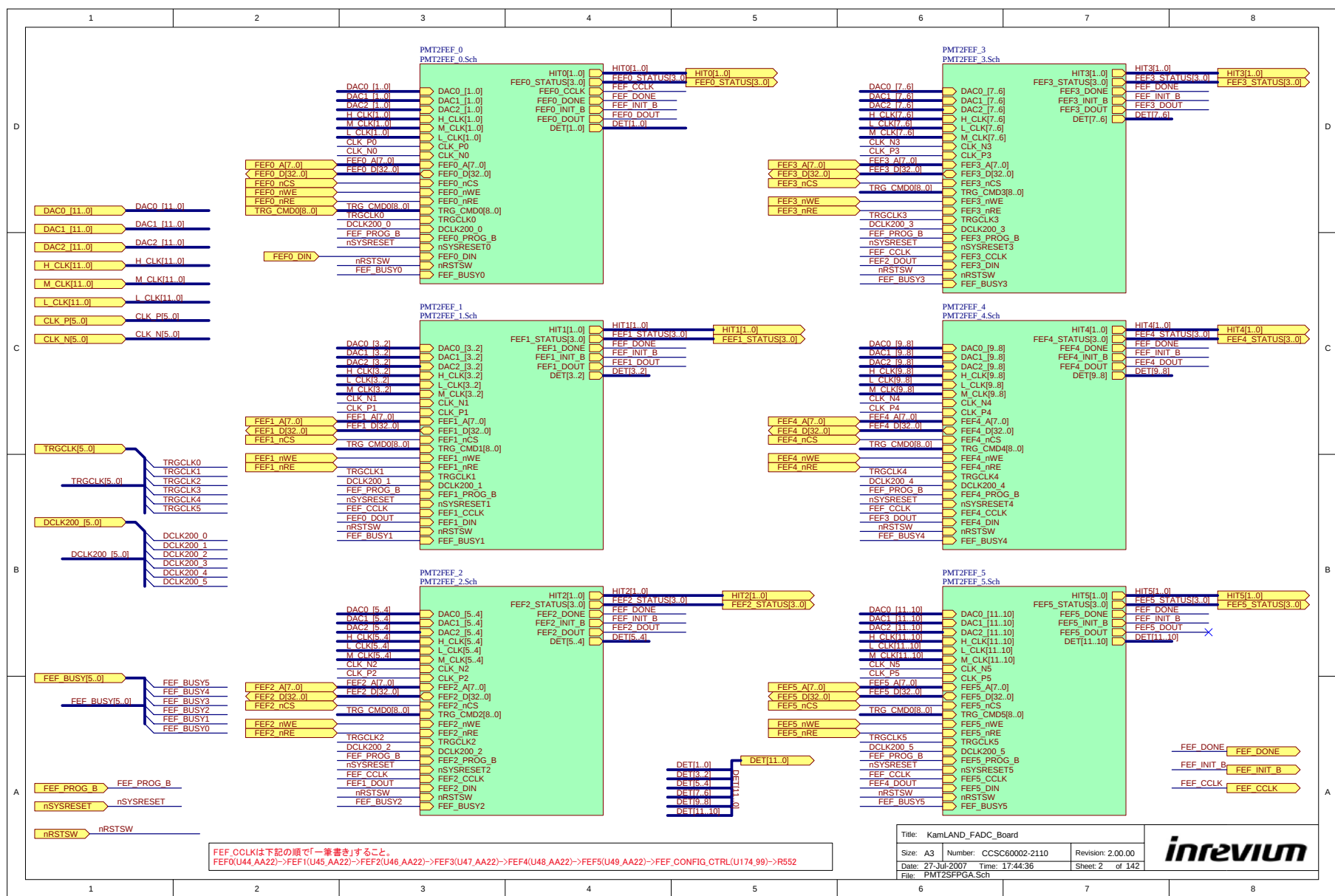
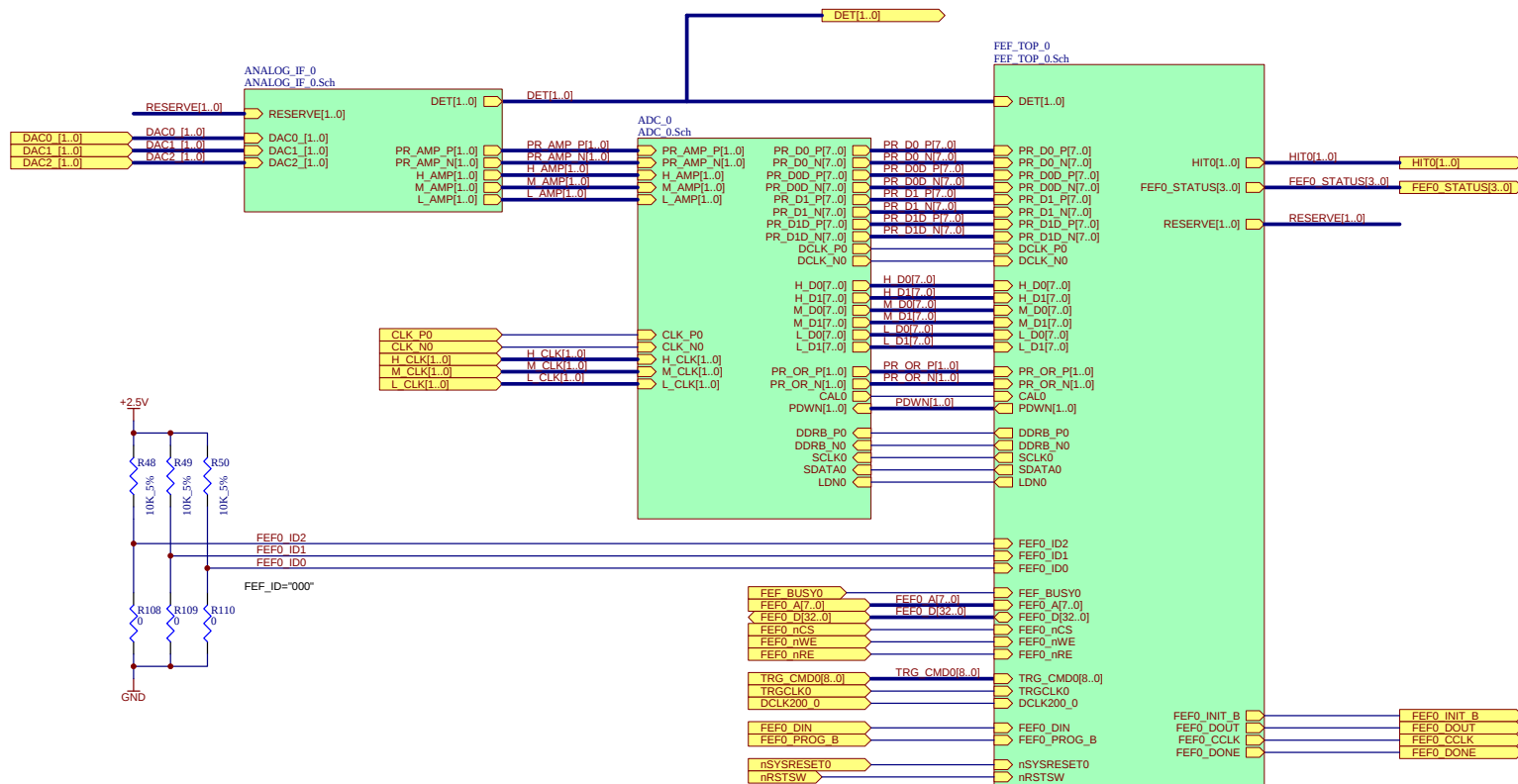
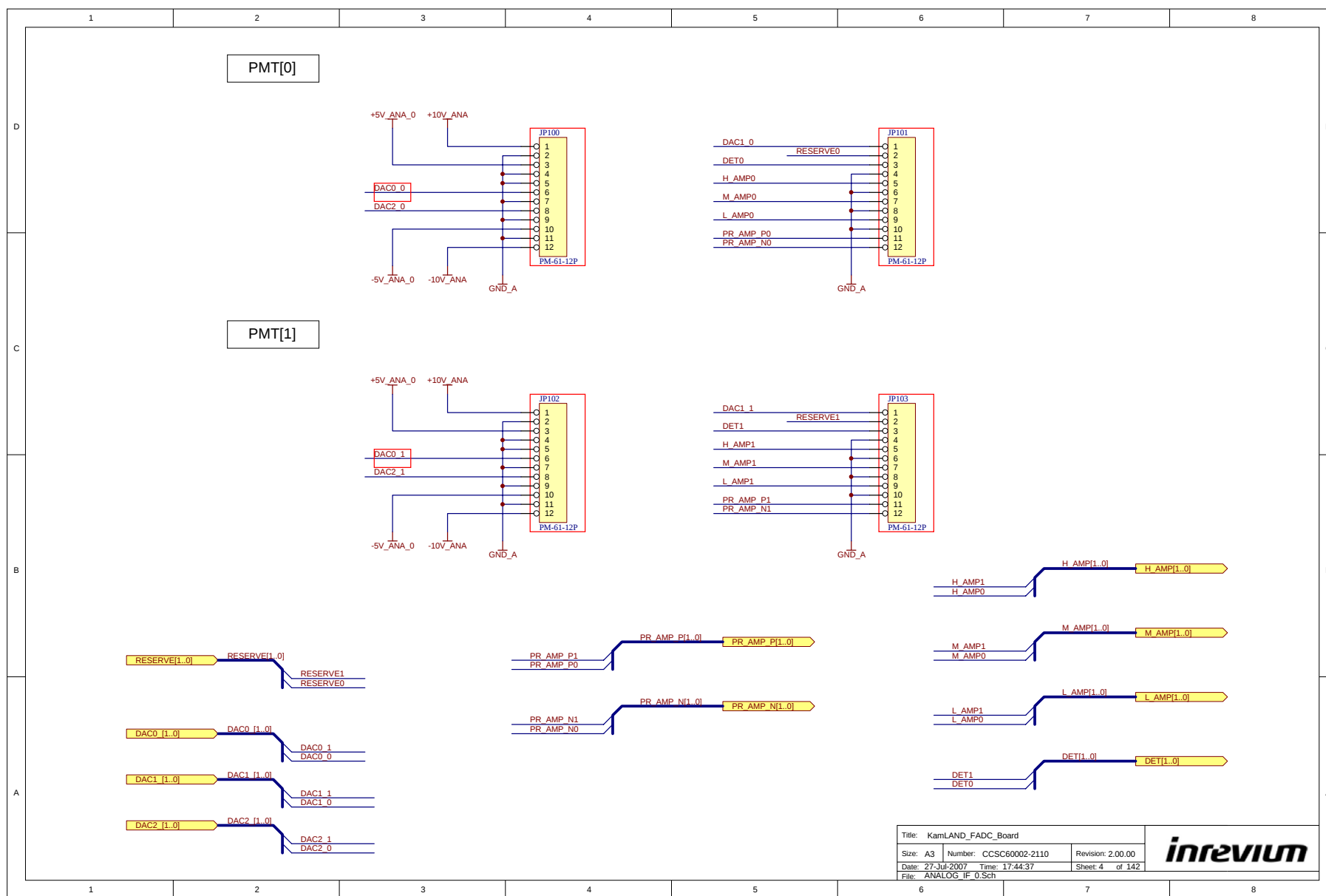


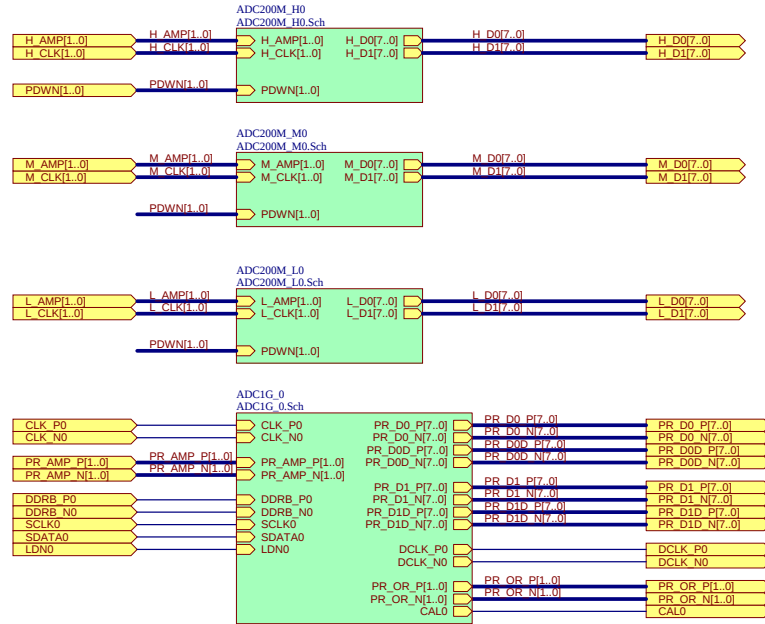


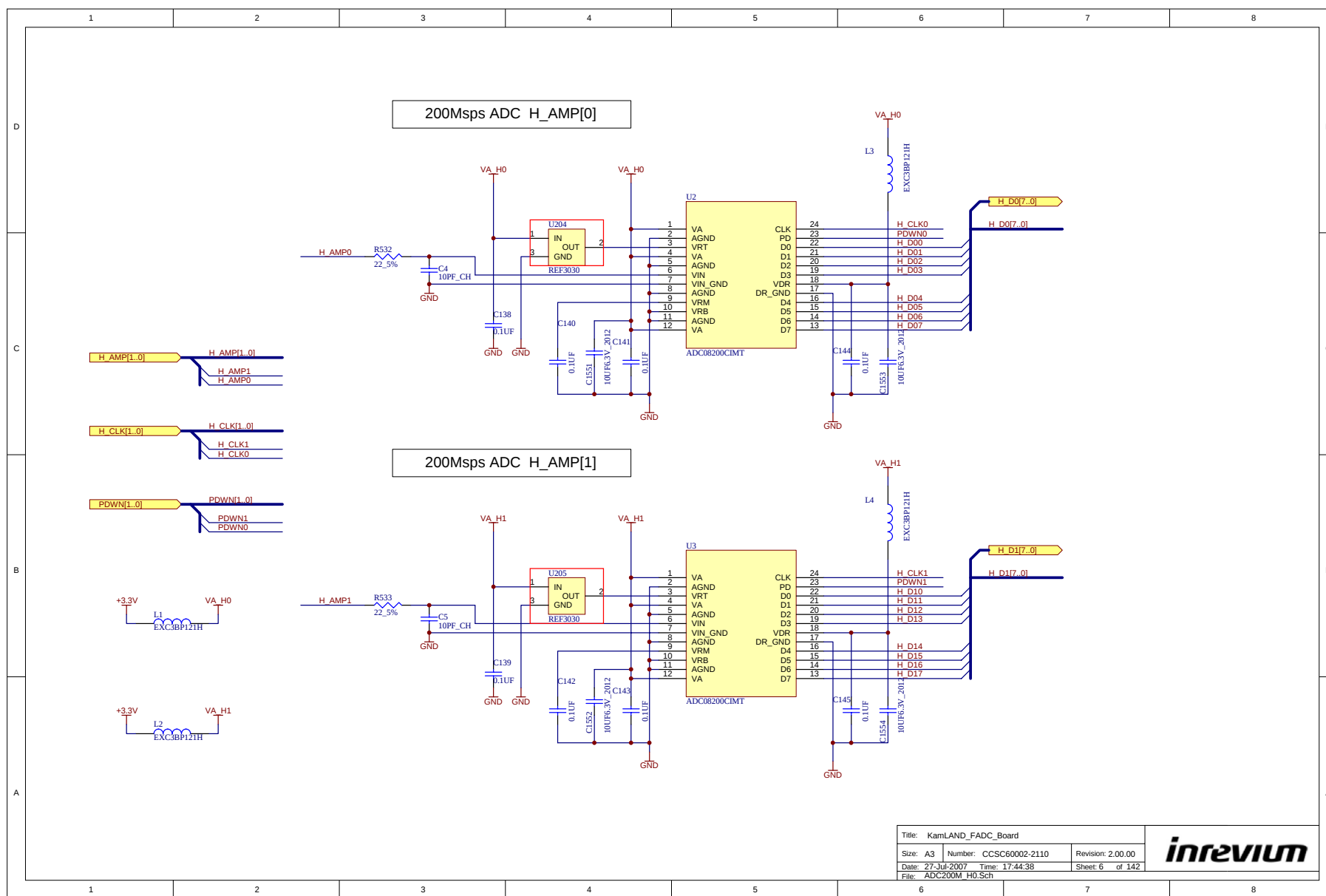
PMT[1..0] to FrontEnd FPGA 0 TOP

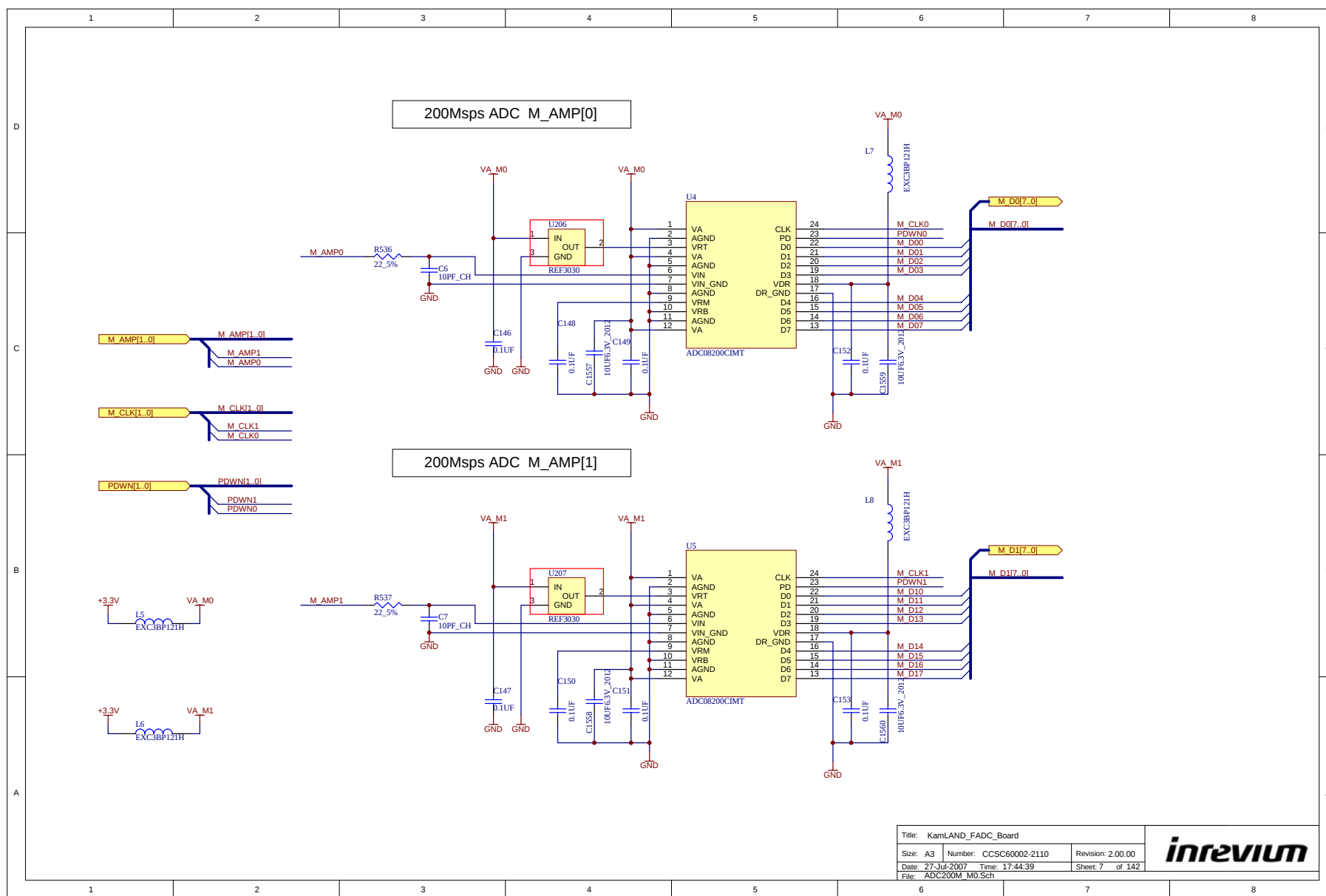


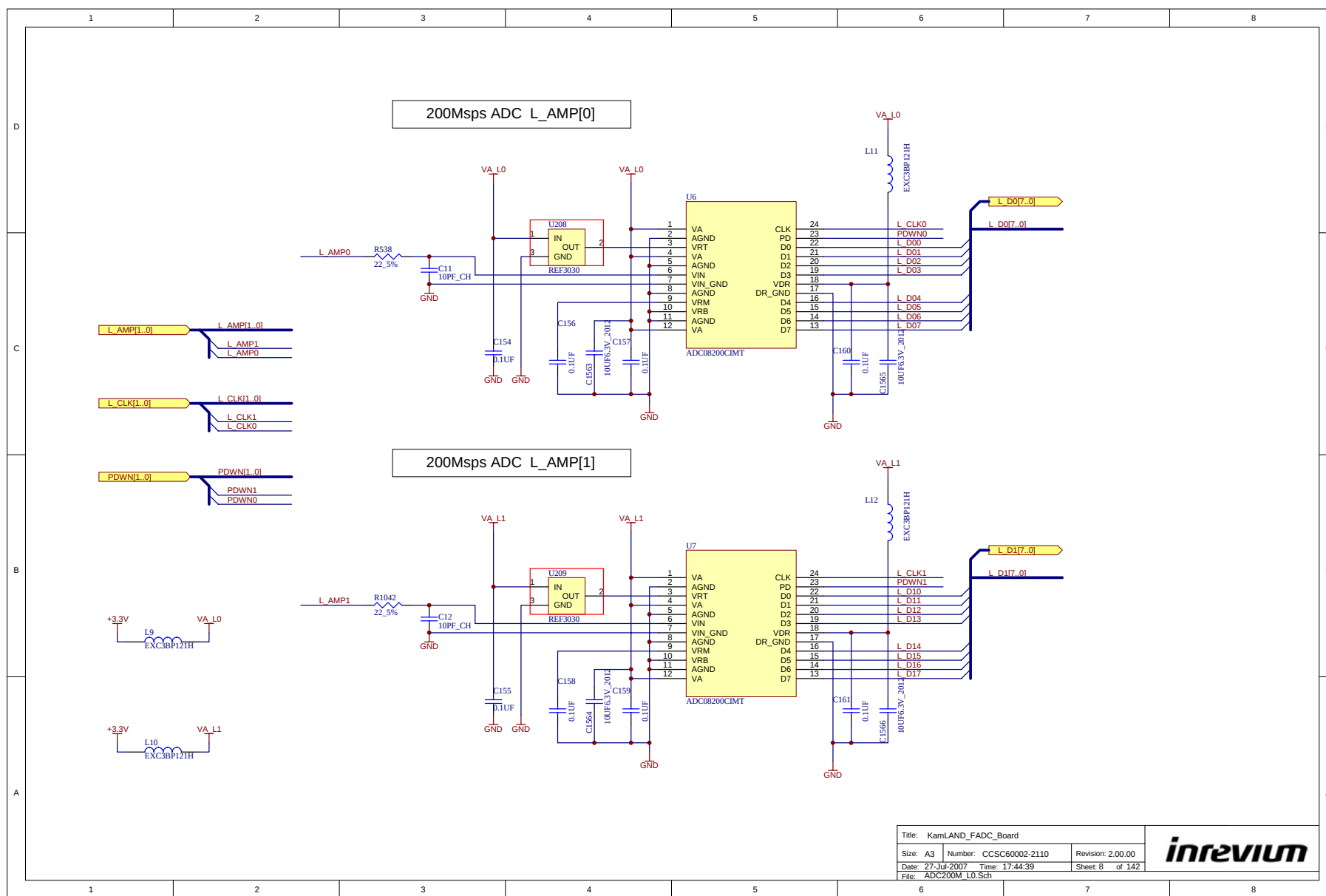


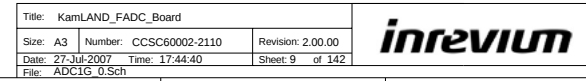
ADC[1..0]
TOP



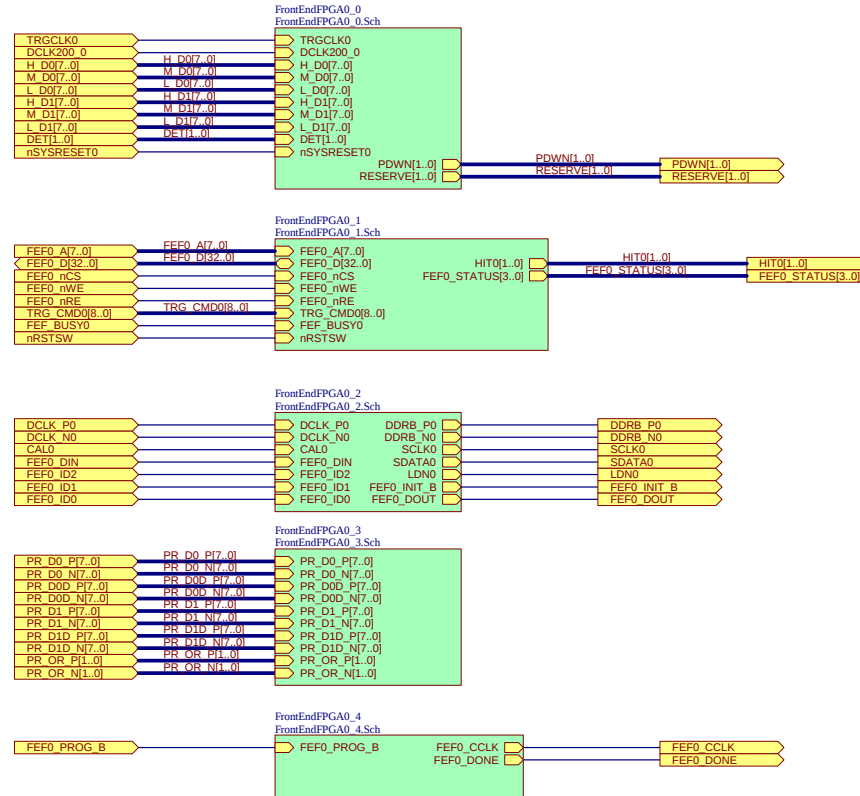


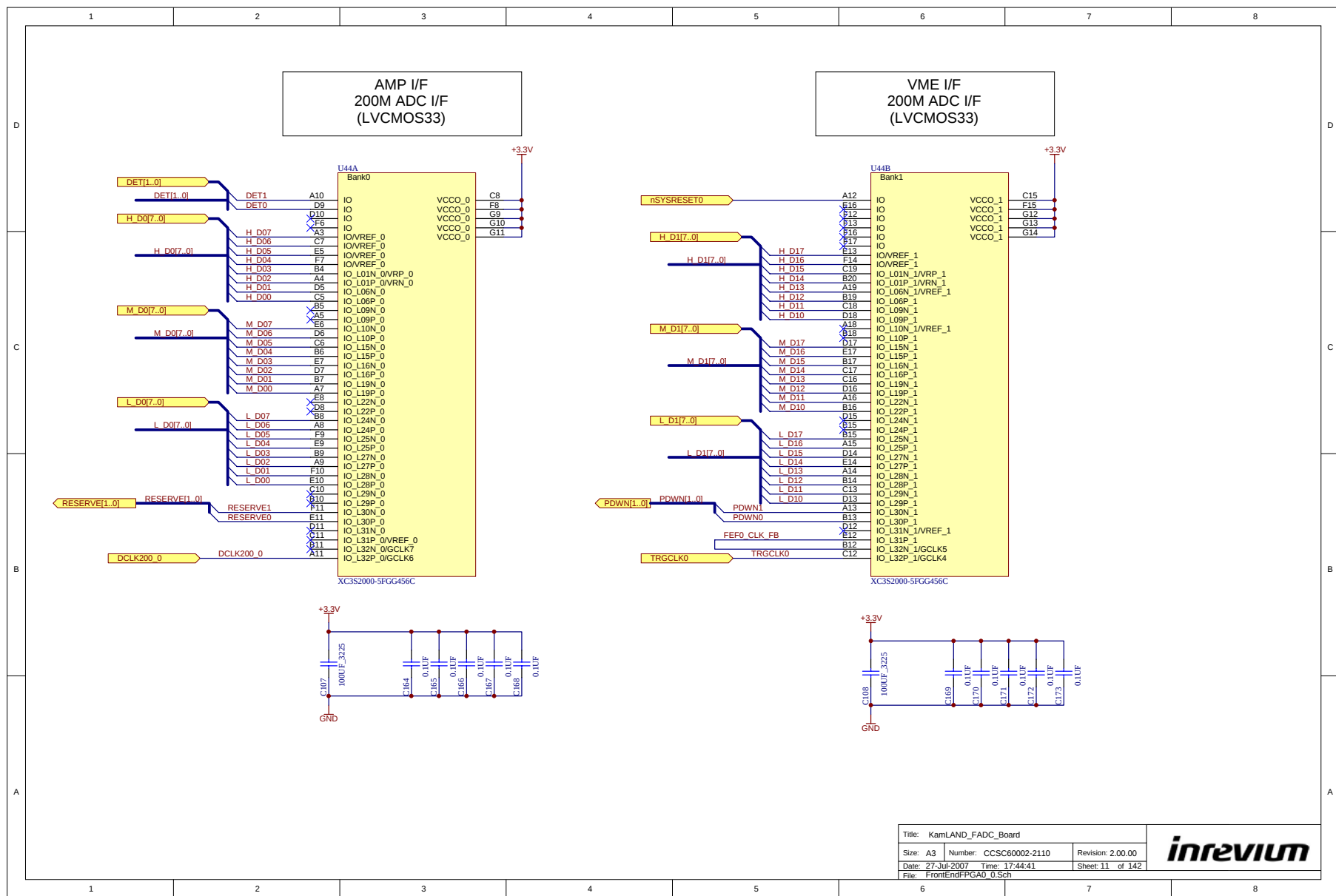


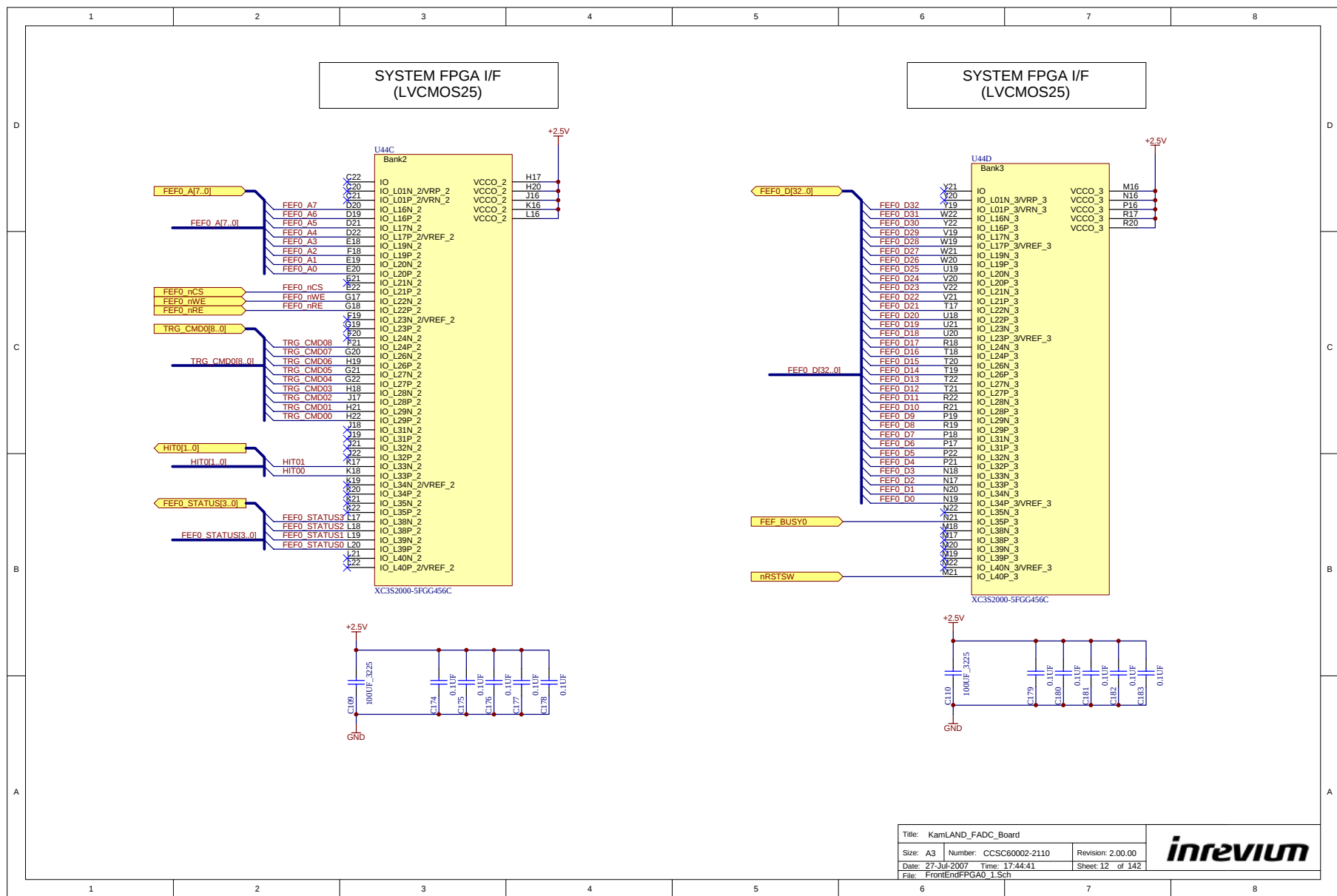


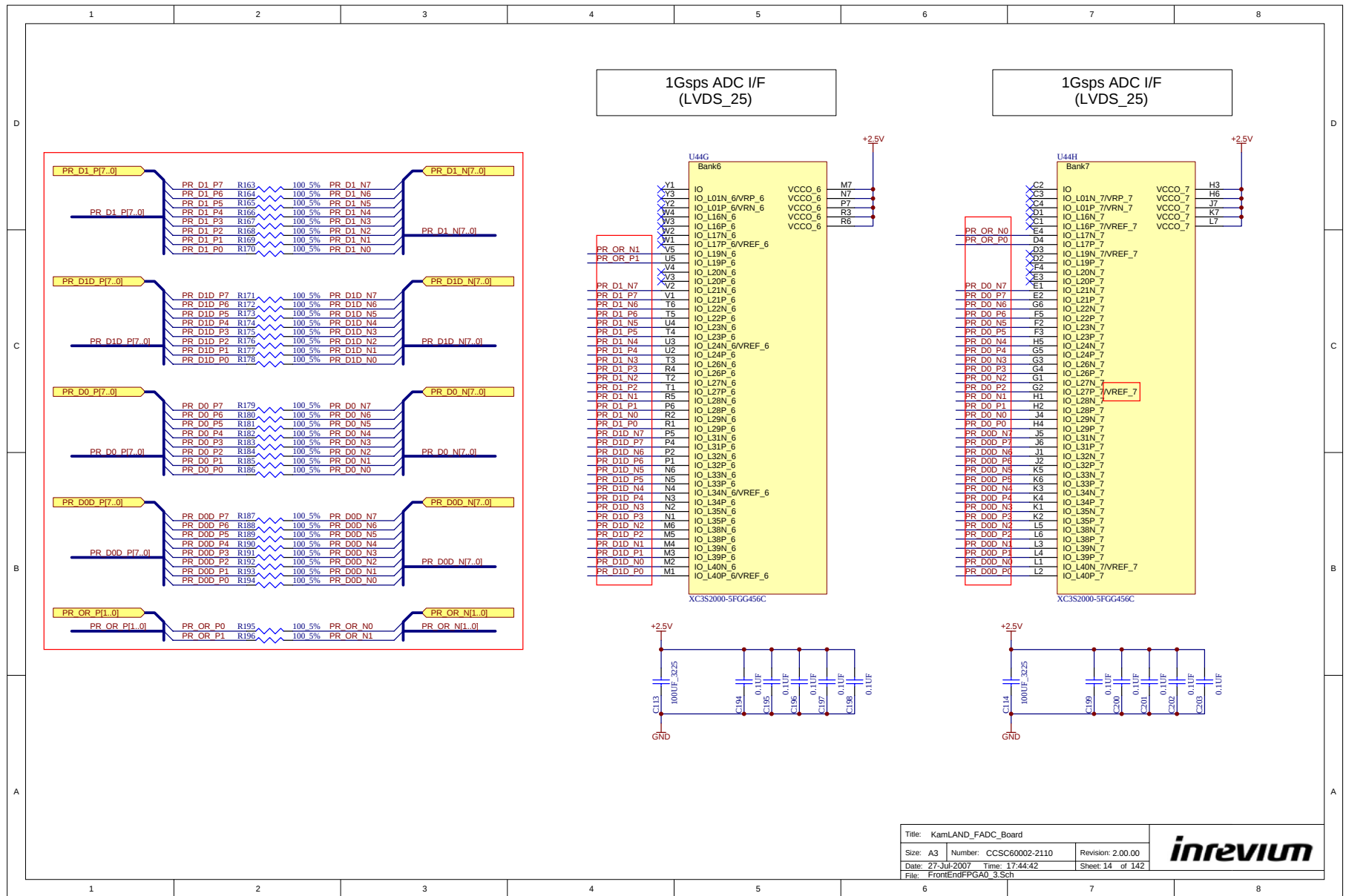


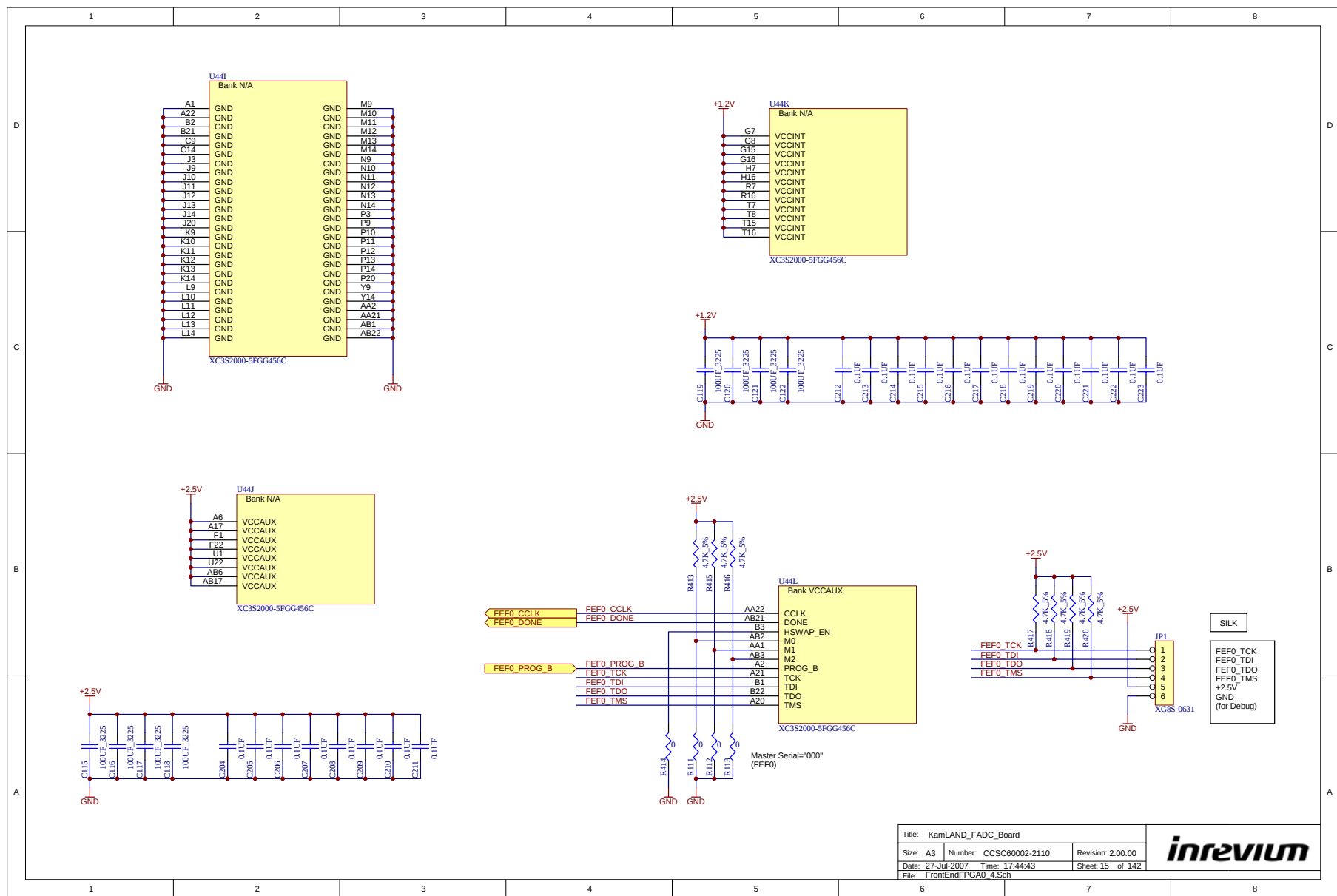
FrontEnd FPGA 0
TOP



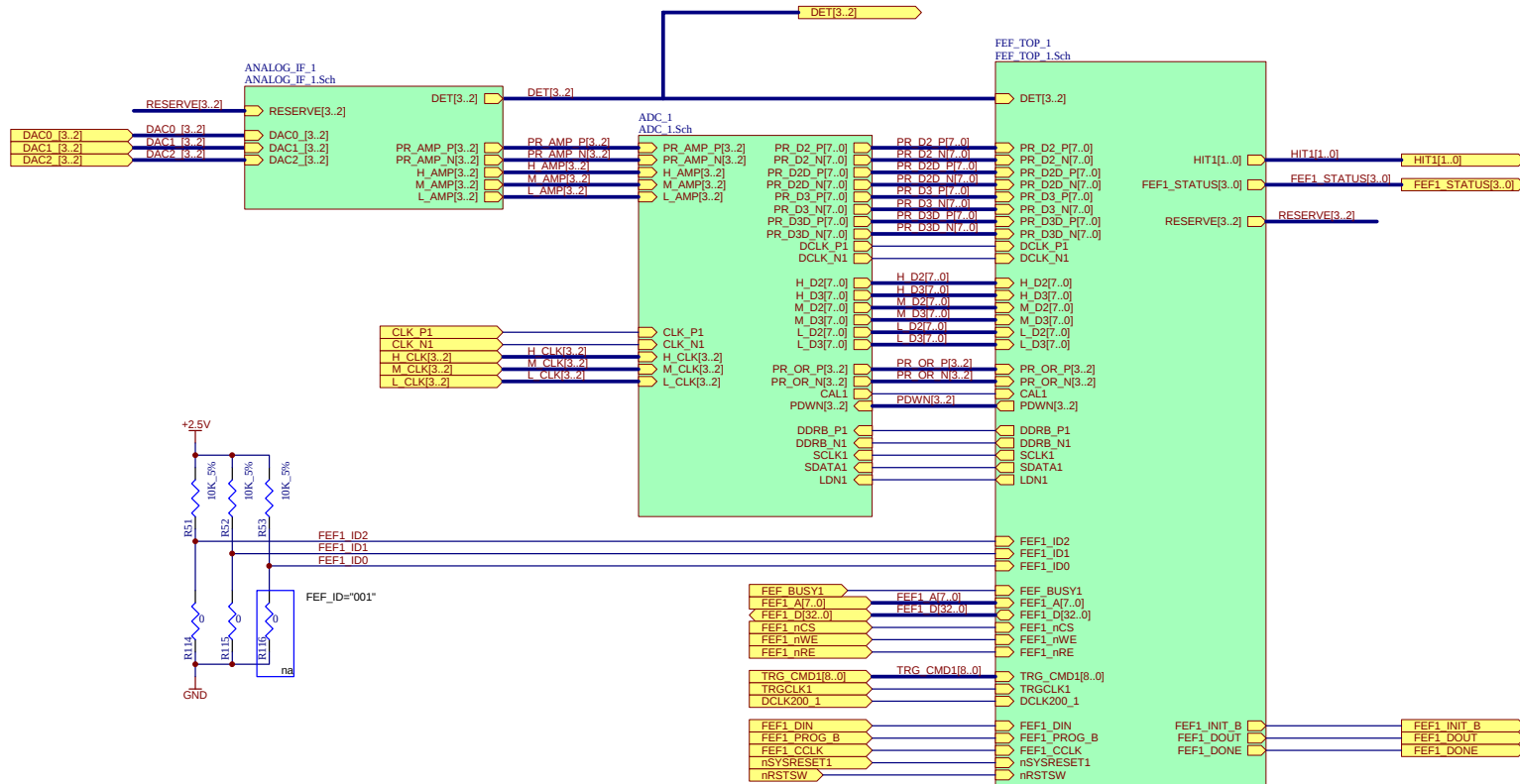


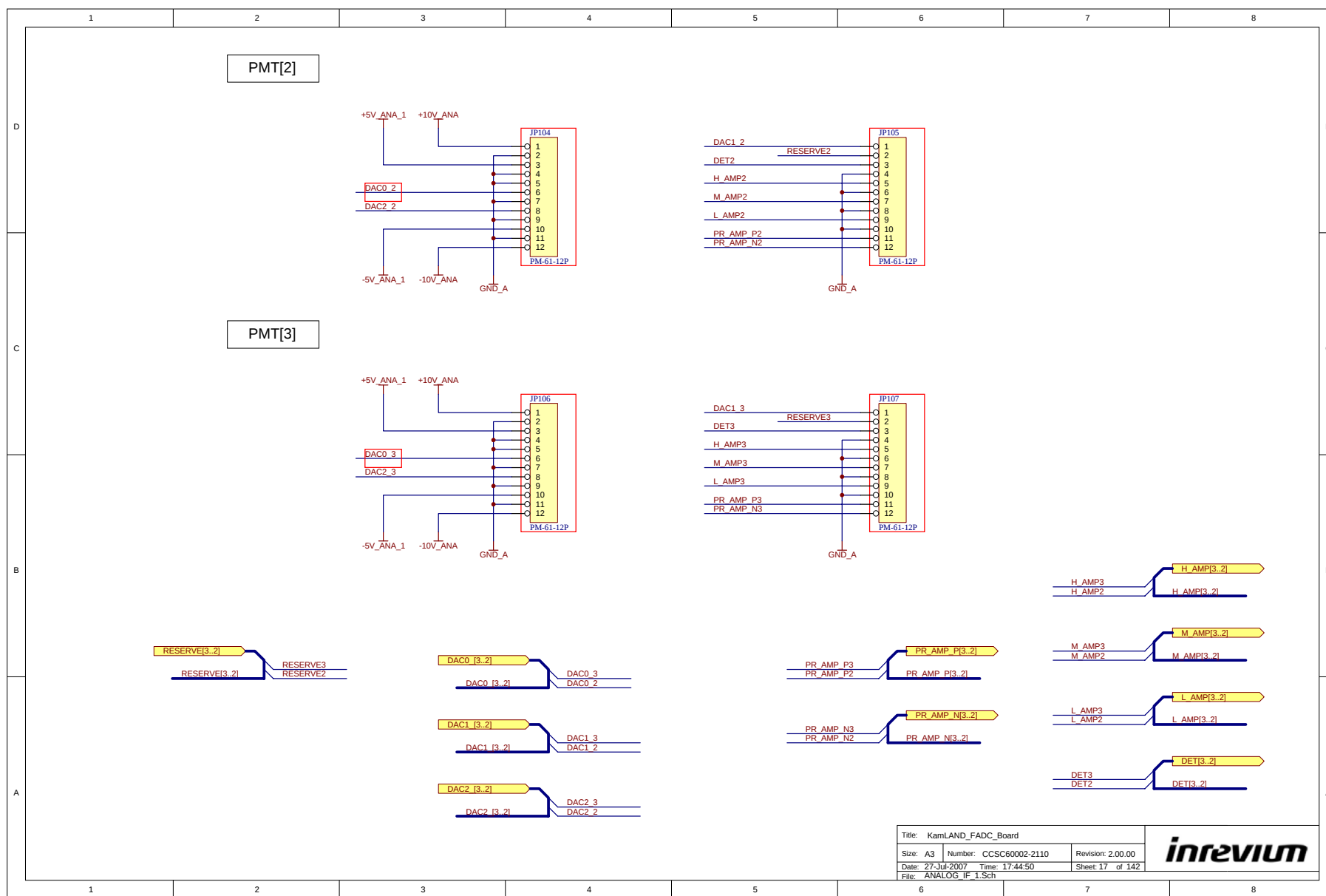




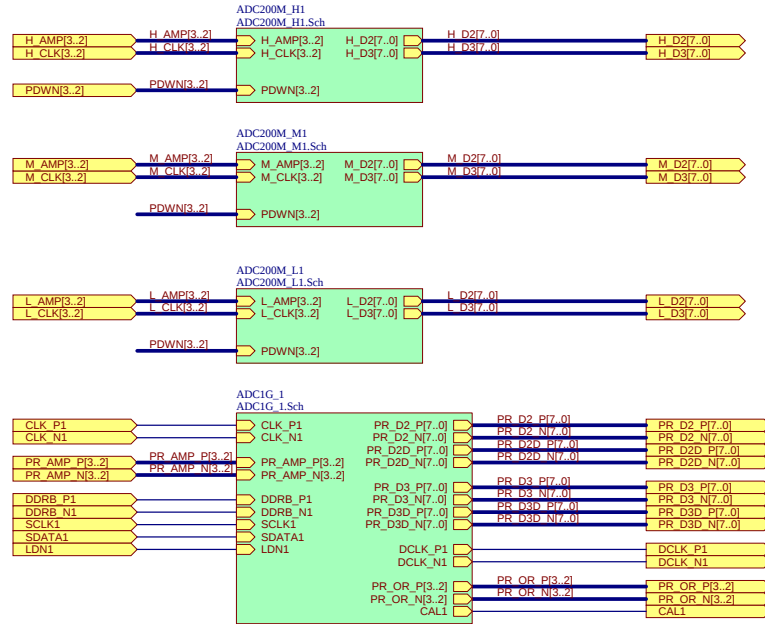


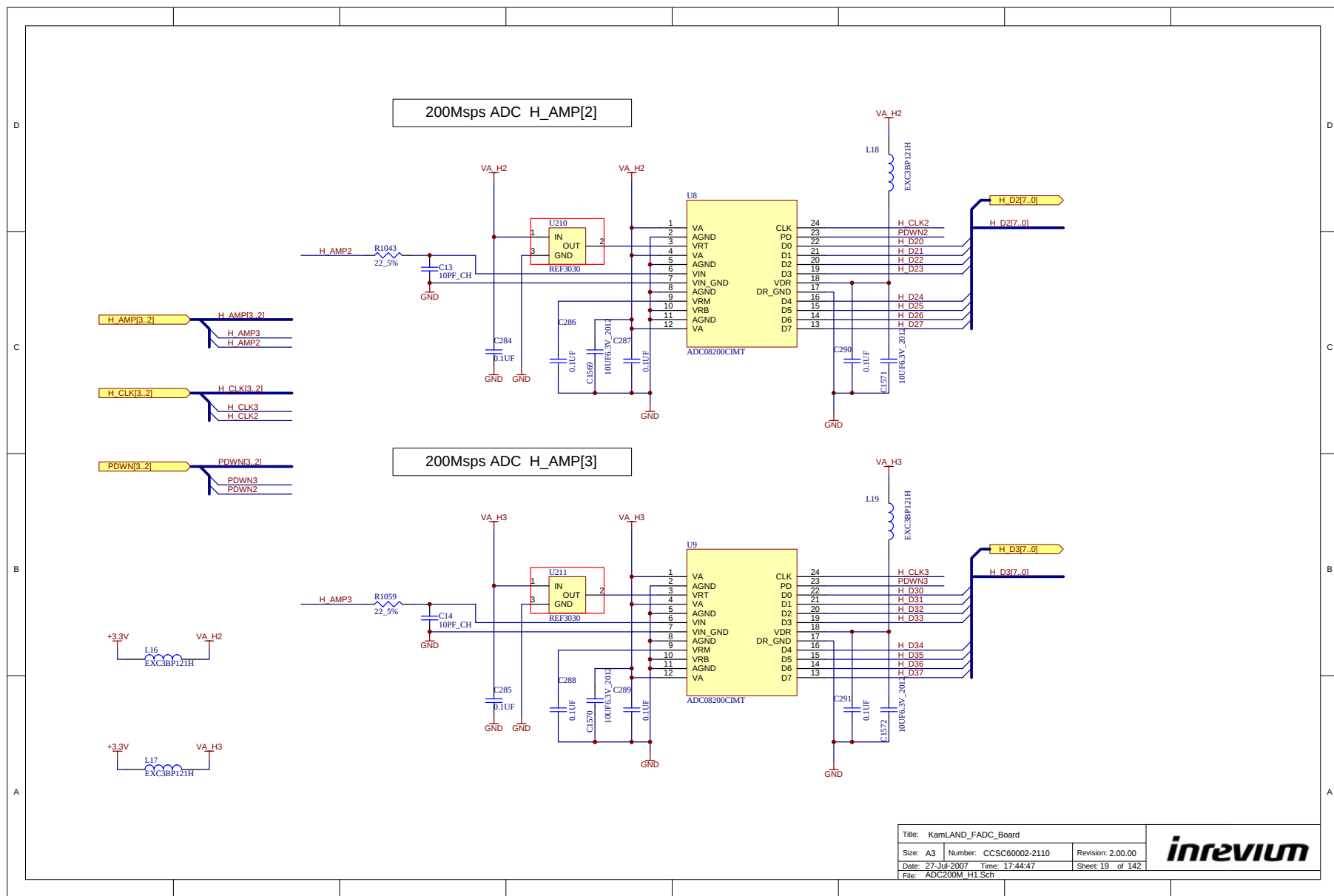
PMT[3..2] to FrontEnd FPGA 1
TOP





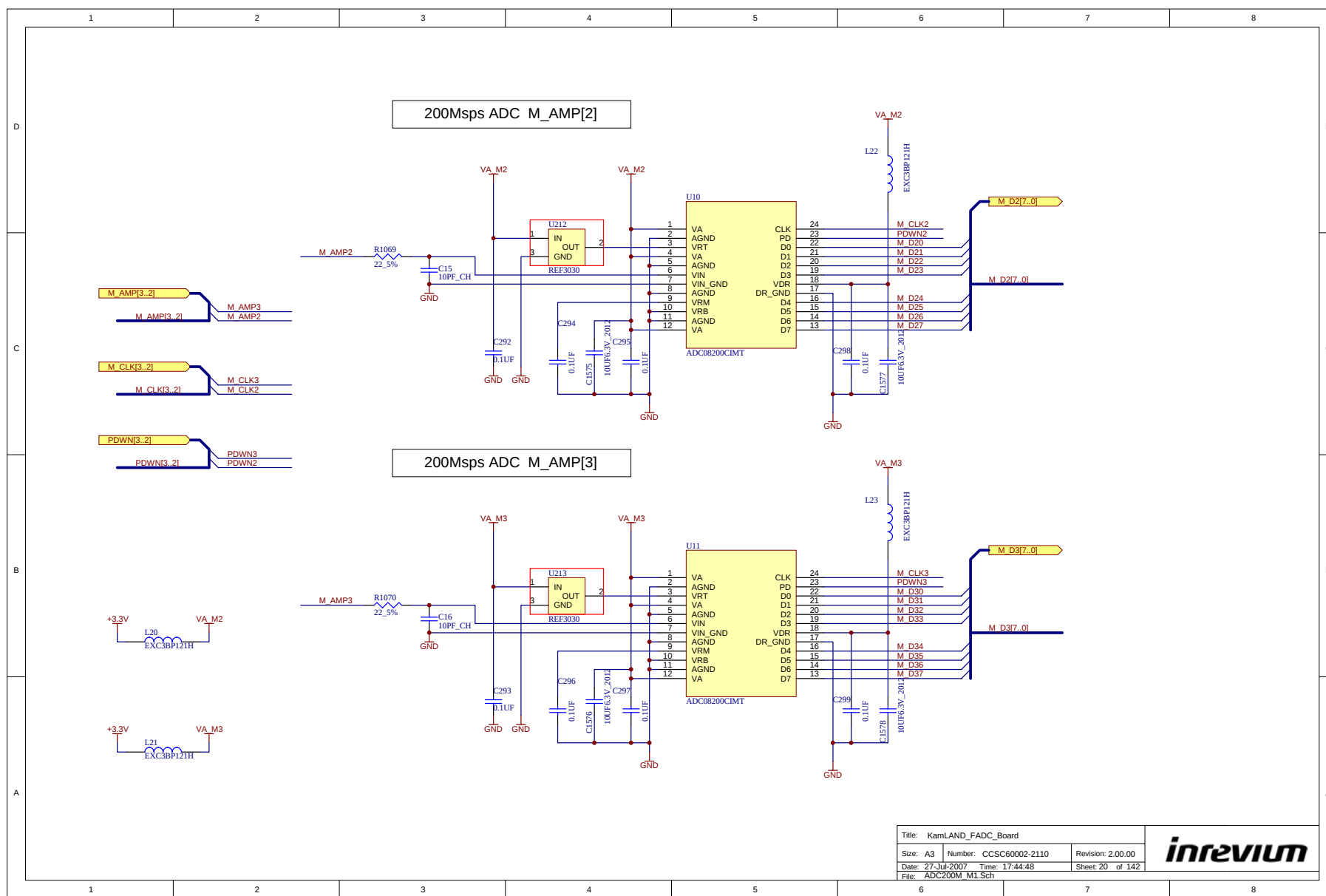
ADC[3..2]
TOP

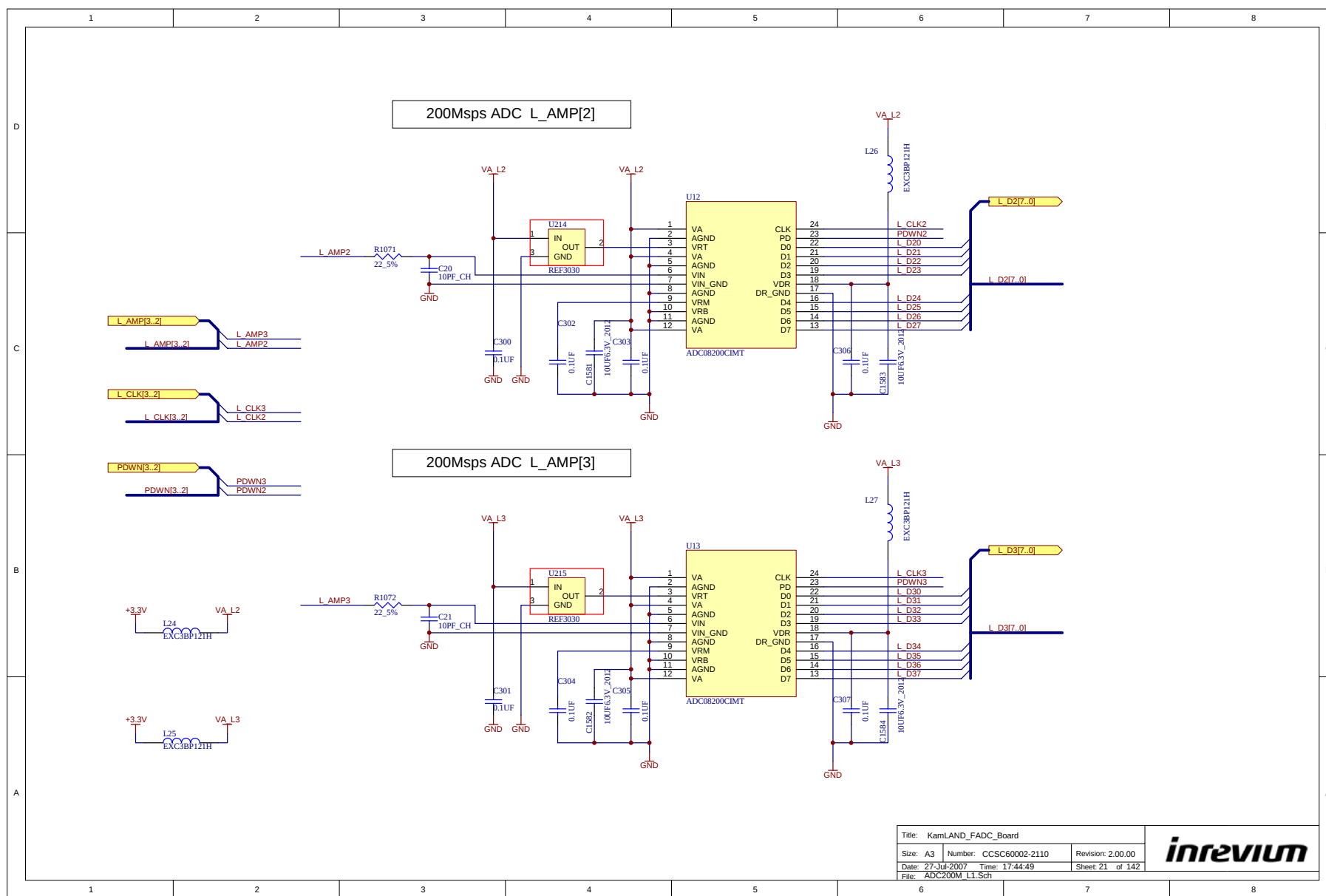




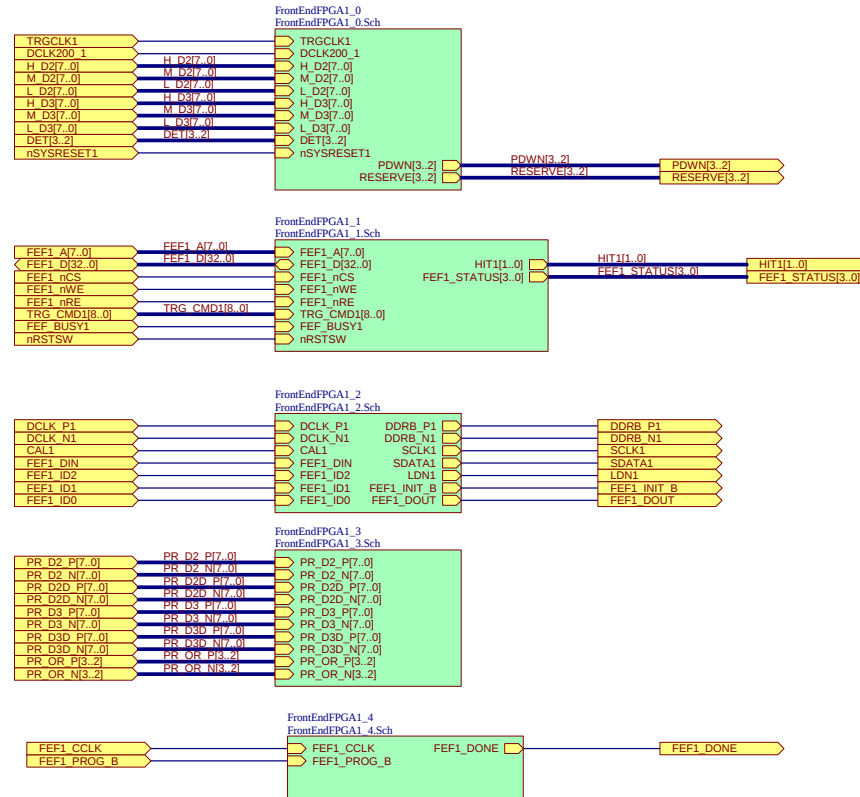
Title: KamLAND_FADC_Board	
Size: A3	Number: CCSC60002-2110
Date: 27-Jul-2007	Time: 17:44:47
File: ADC200M_H1.Sch	Revision: 2.00.00
	Sheet: 19 of 142

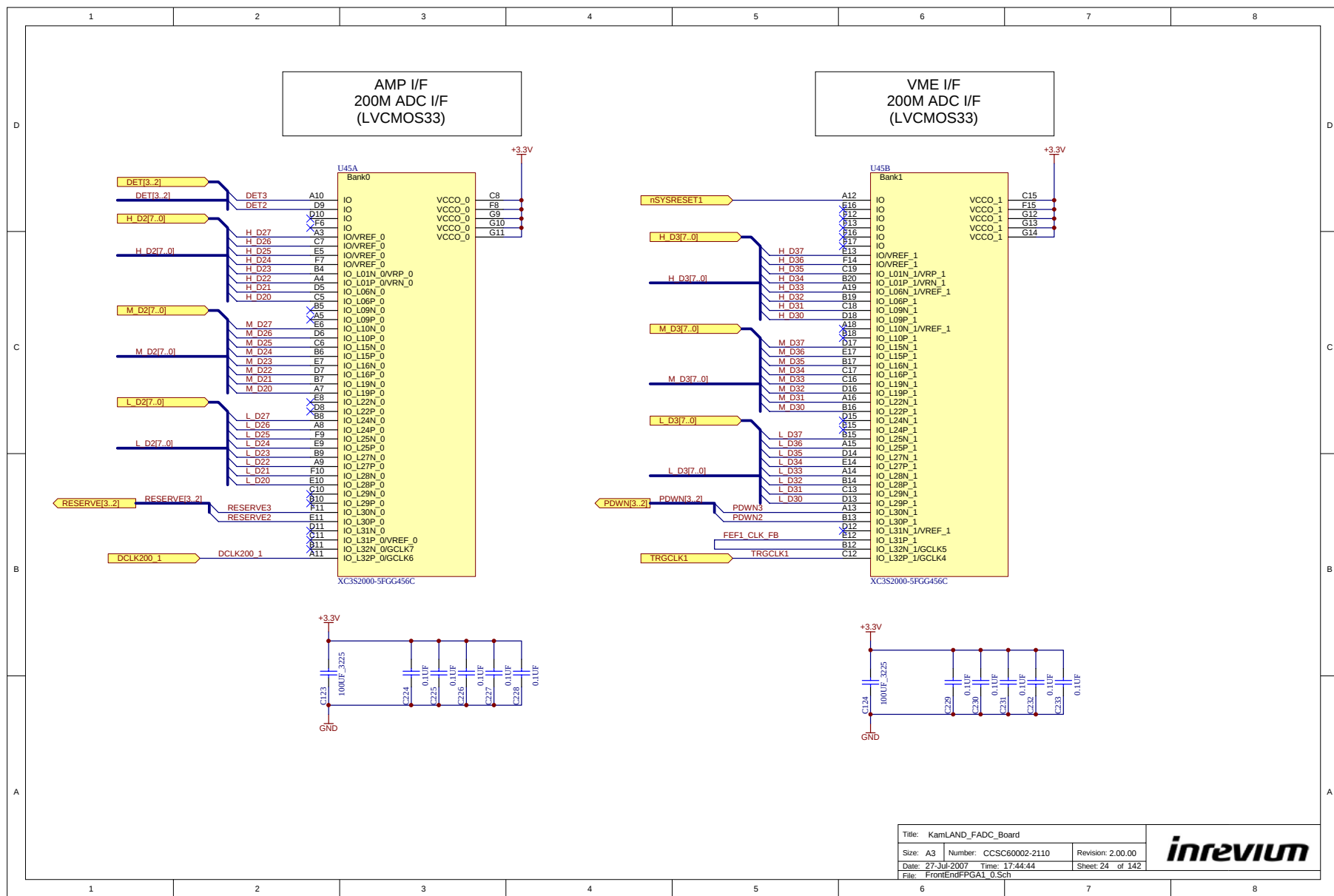
inrevium

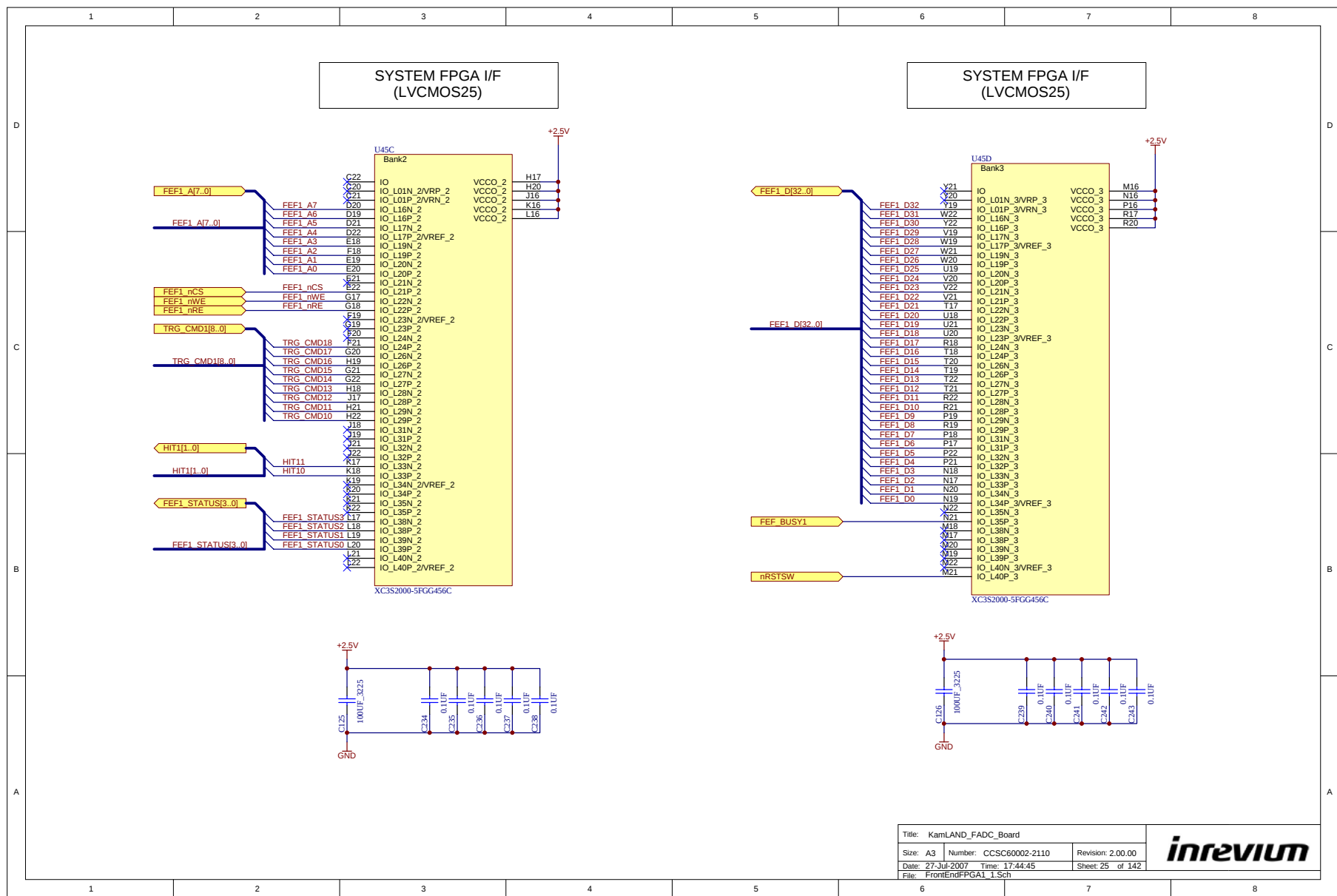


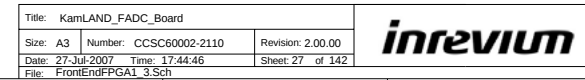


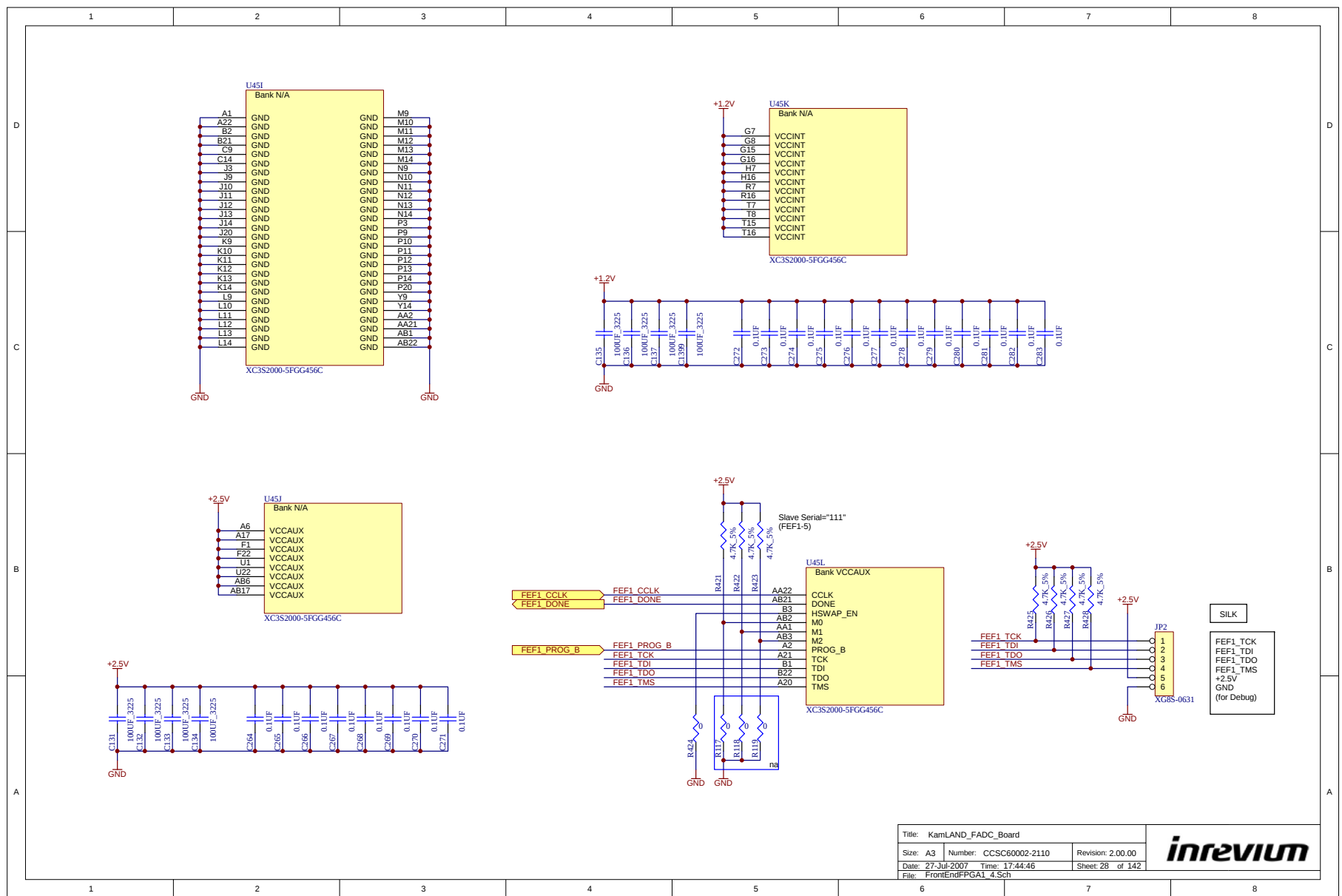
FrontEnd FPGA 1 TOP



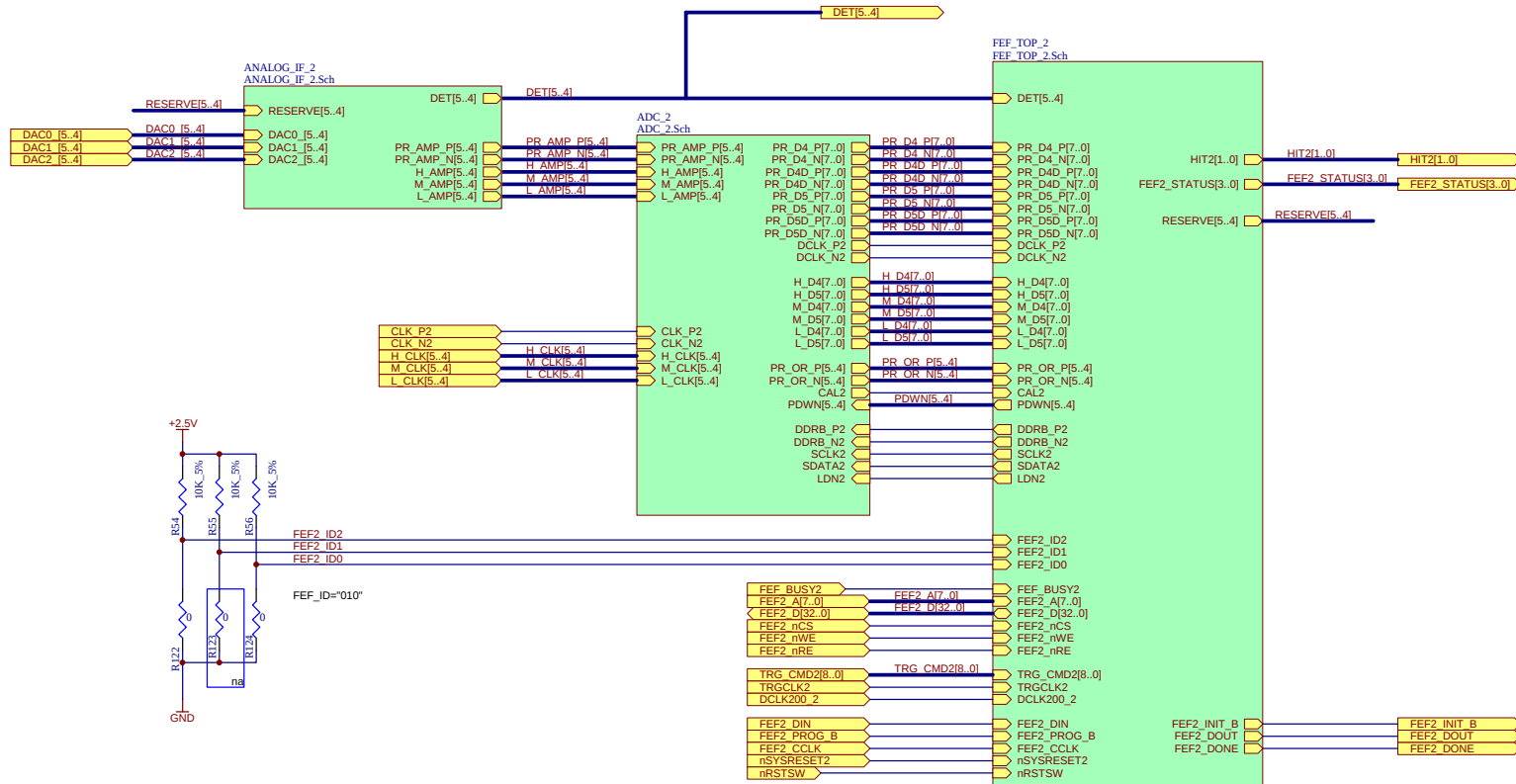


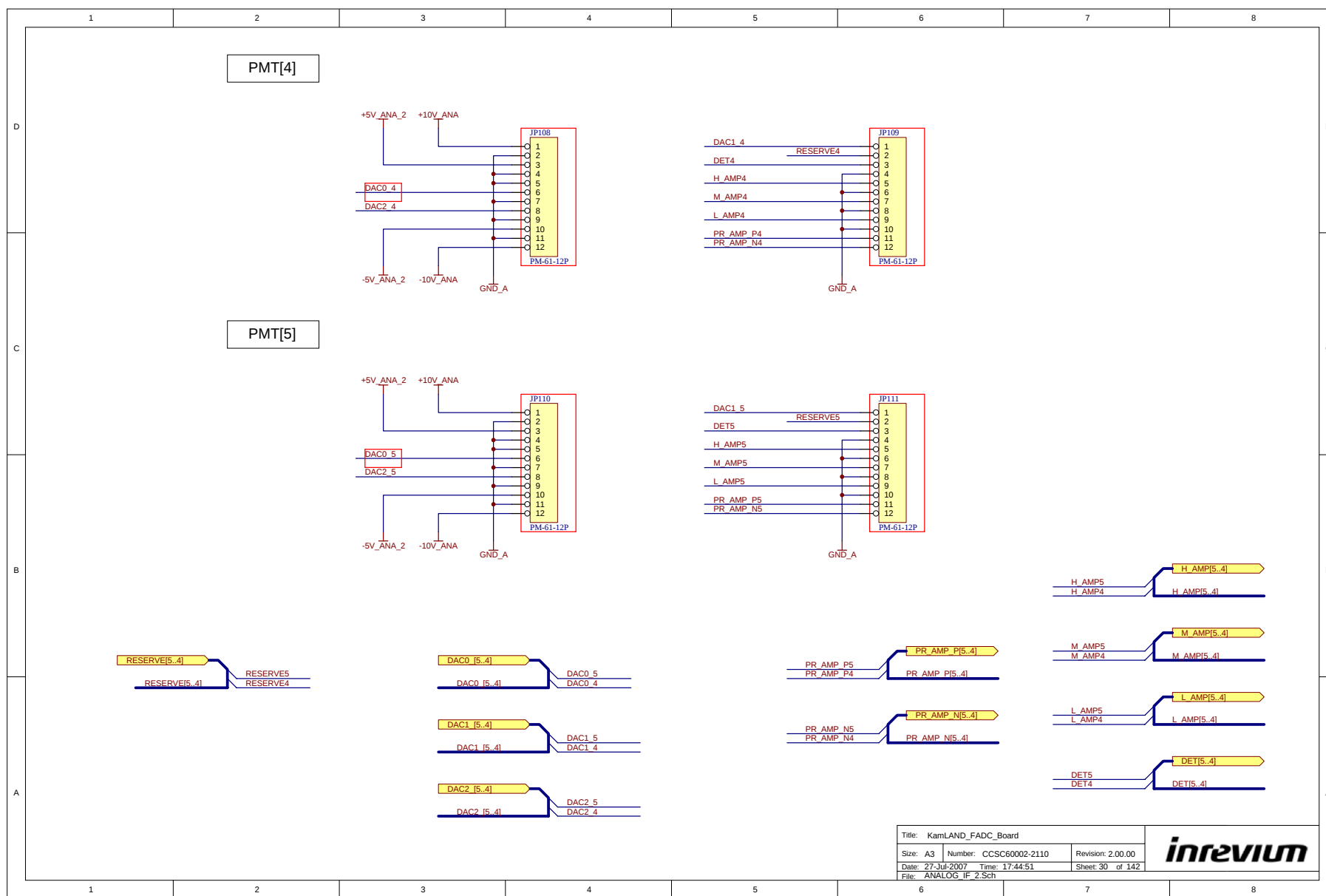




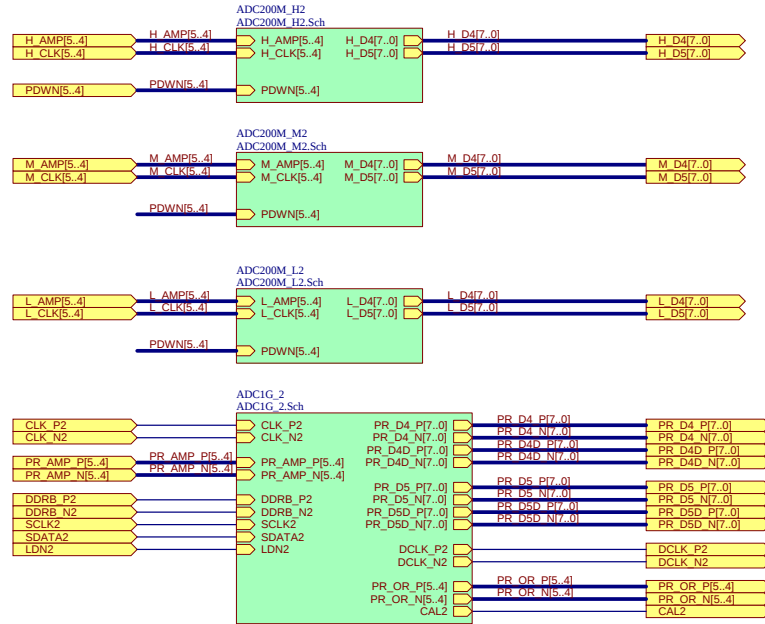


PMT[5..4] to FrontEnd FPGA 2 TOP



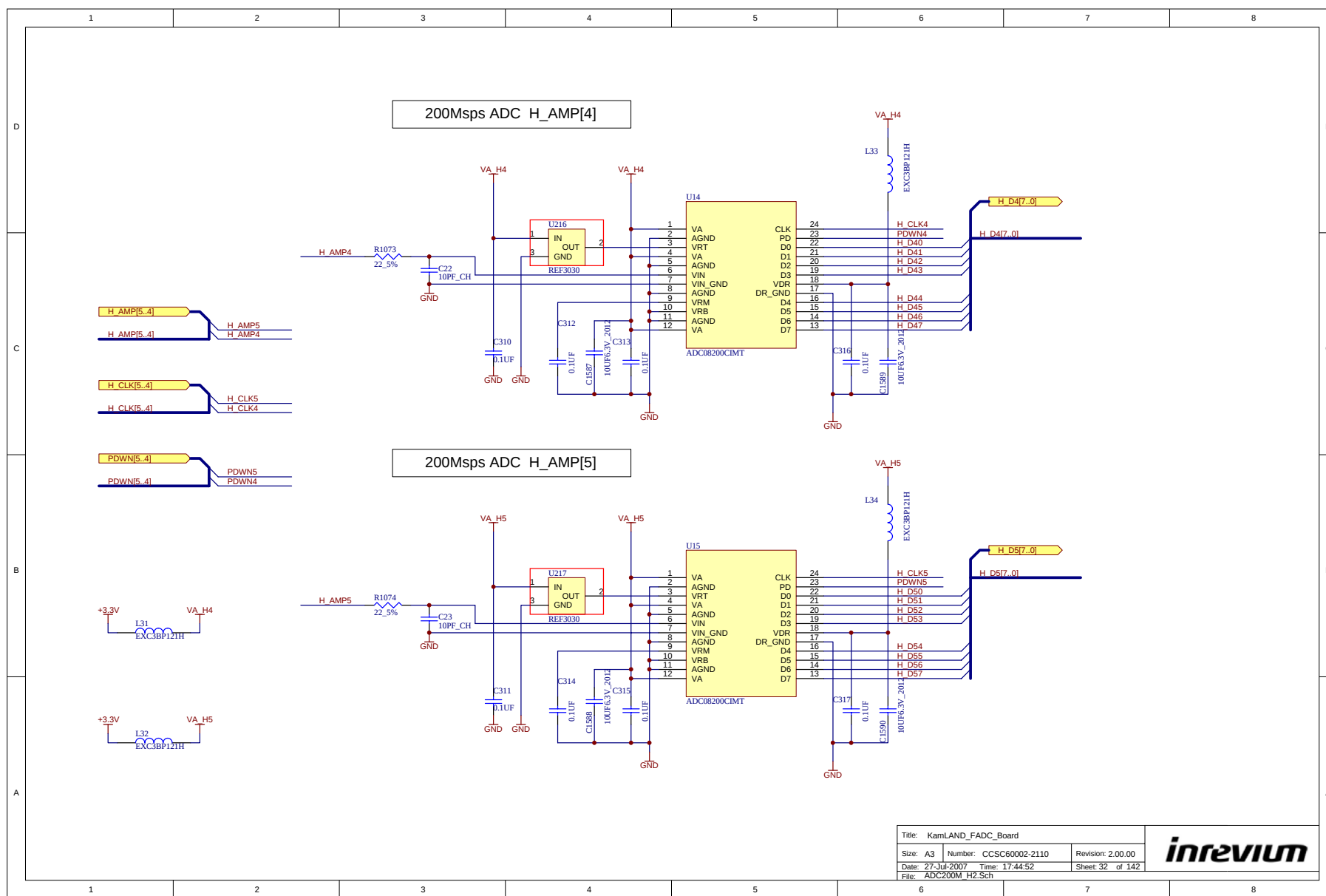


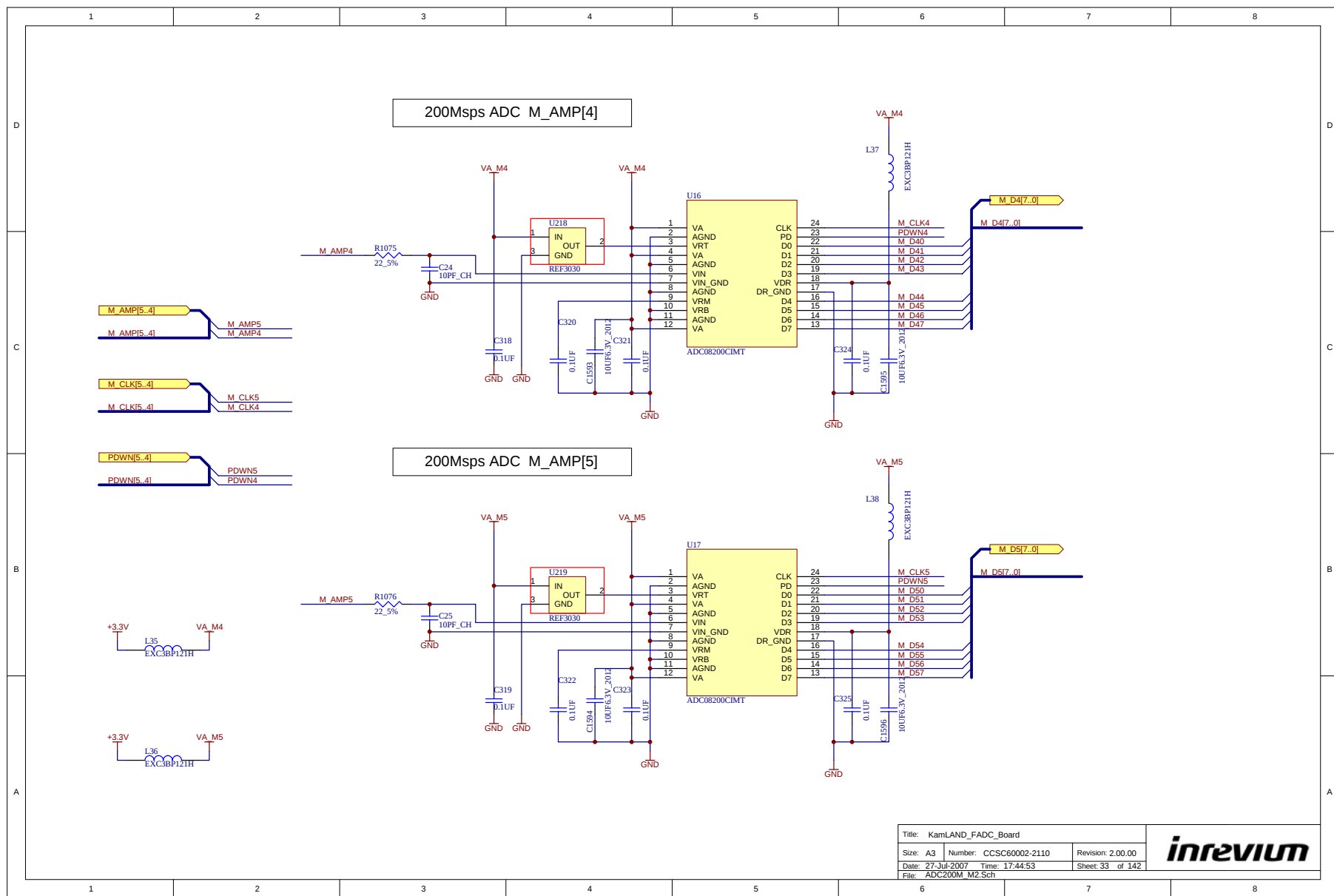
ADC[5..4]
TOP

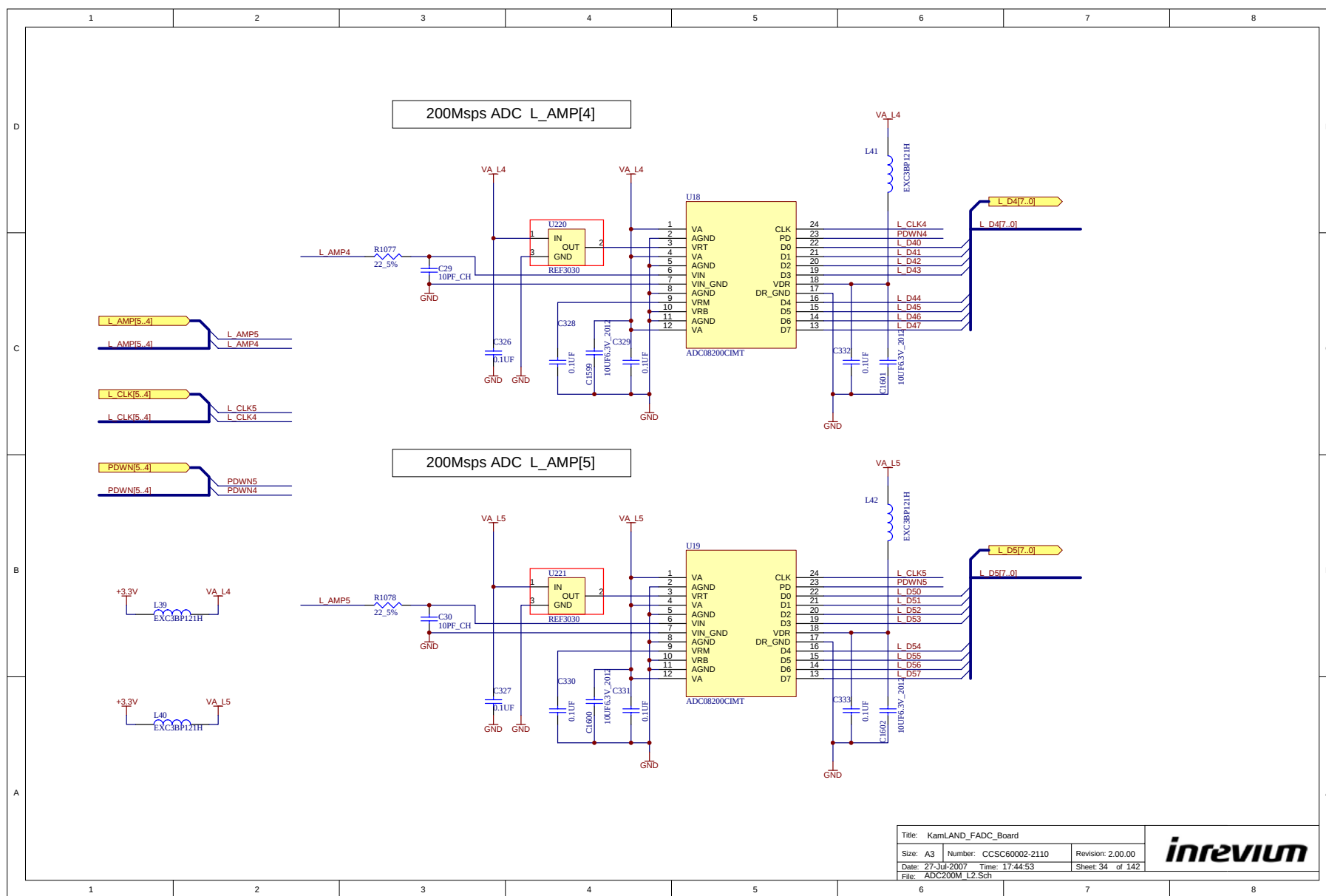


Title: KamLAND_FADC_Board		
Size: A3	Number: CCSC60002-2110	Revision: 2.00.00
Date: 27-Jul-2007	Time: 17:44:52	Sheet: 31 of 142
File: ADC_2.Sch		

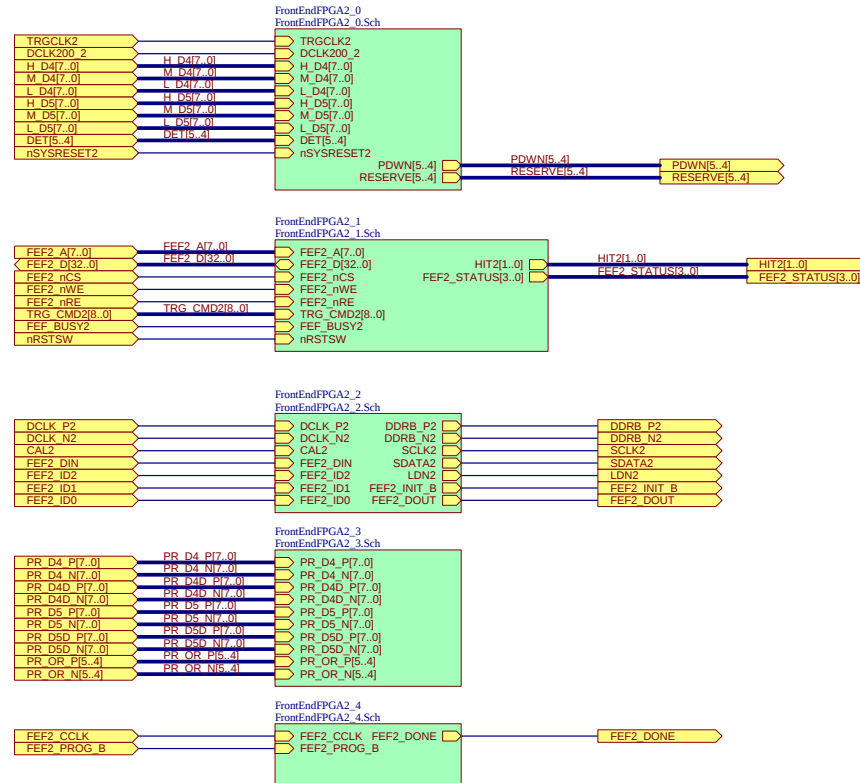
inrevium

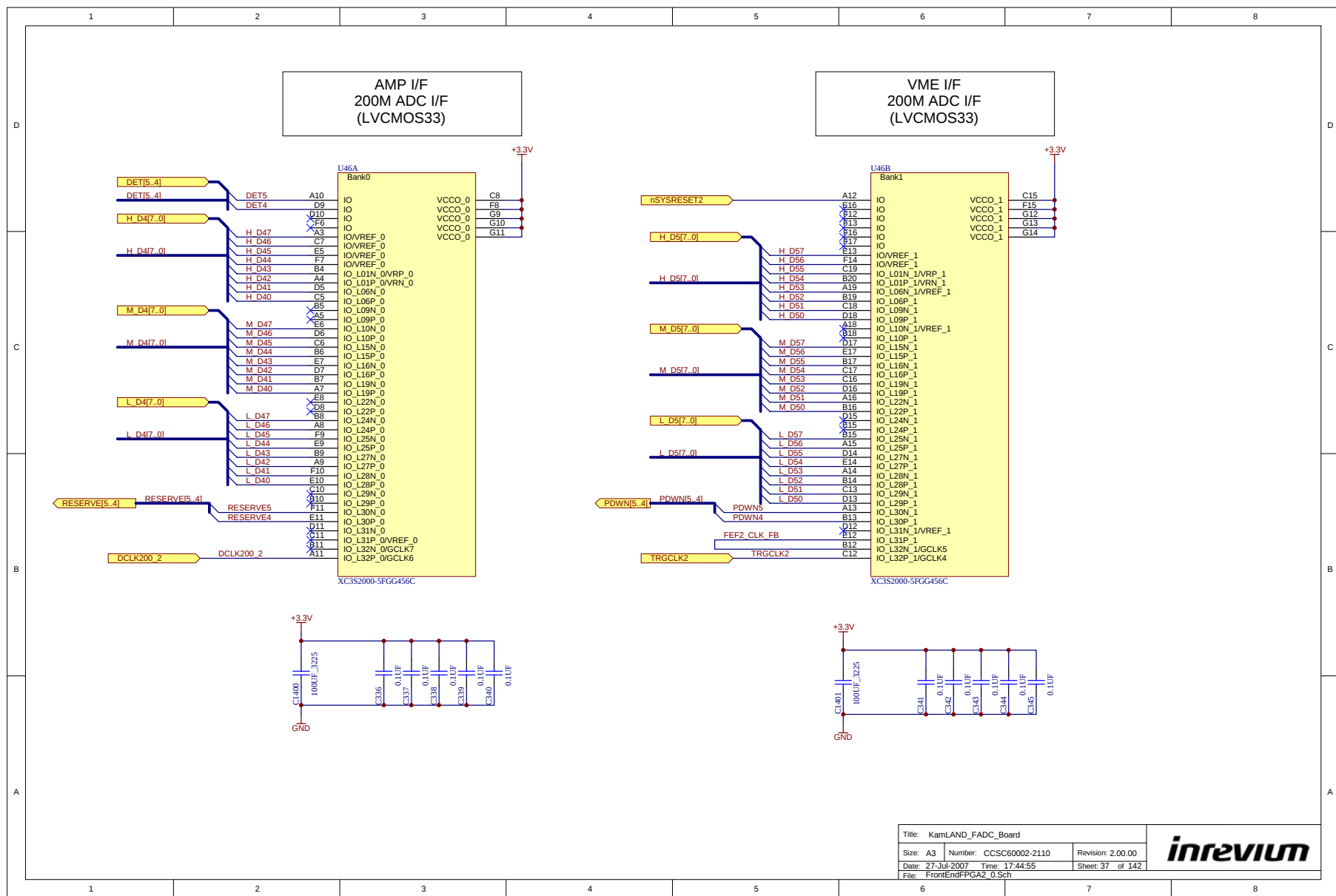


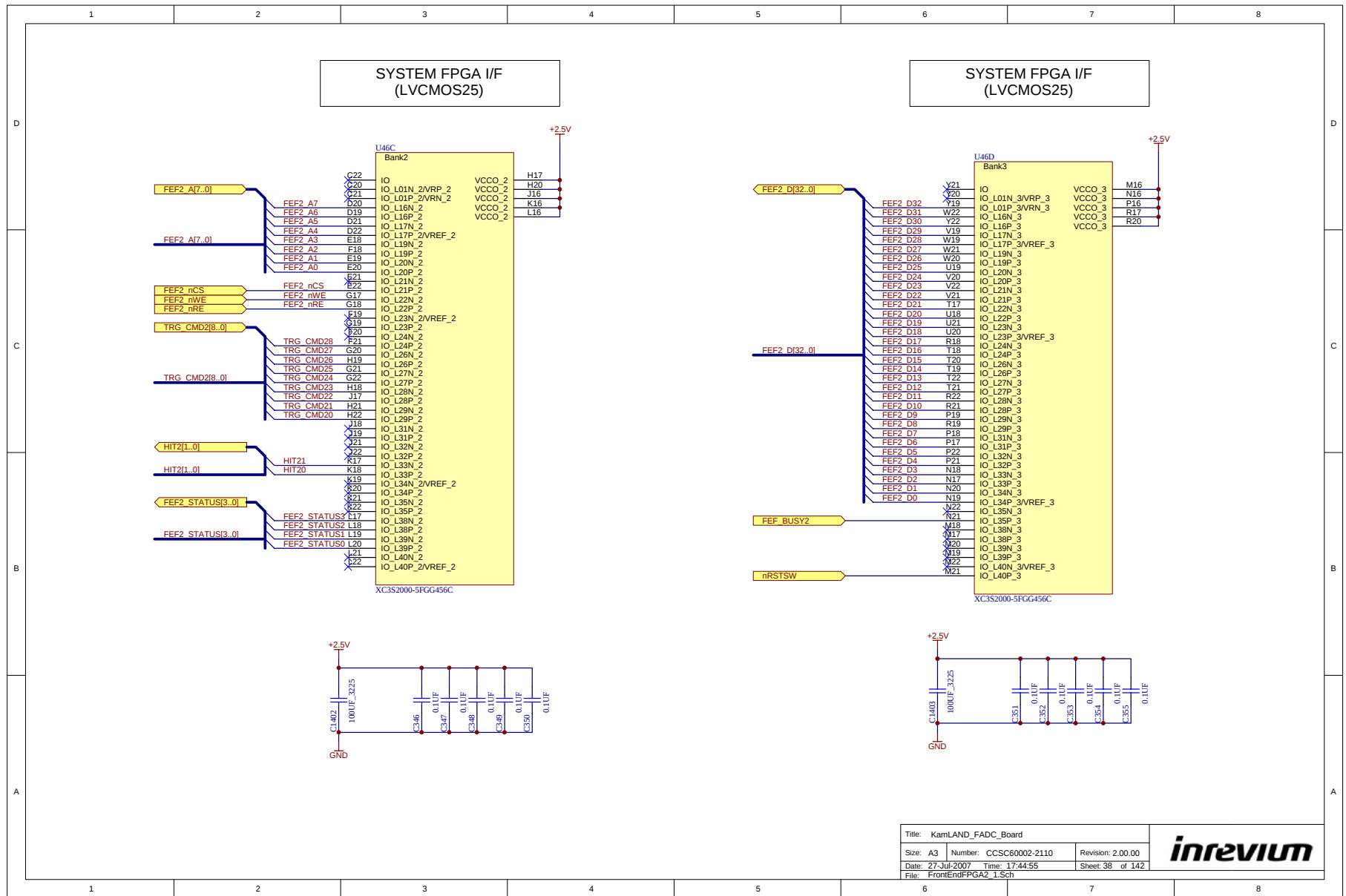


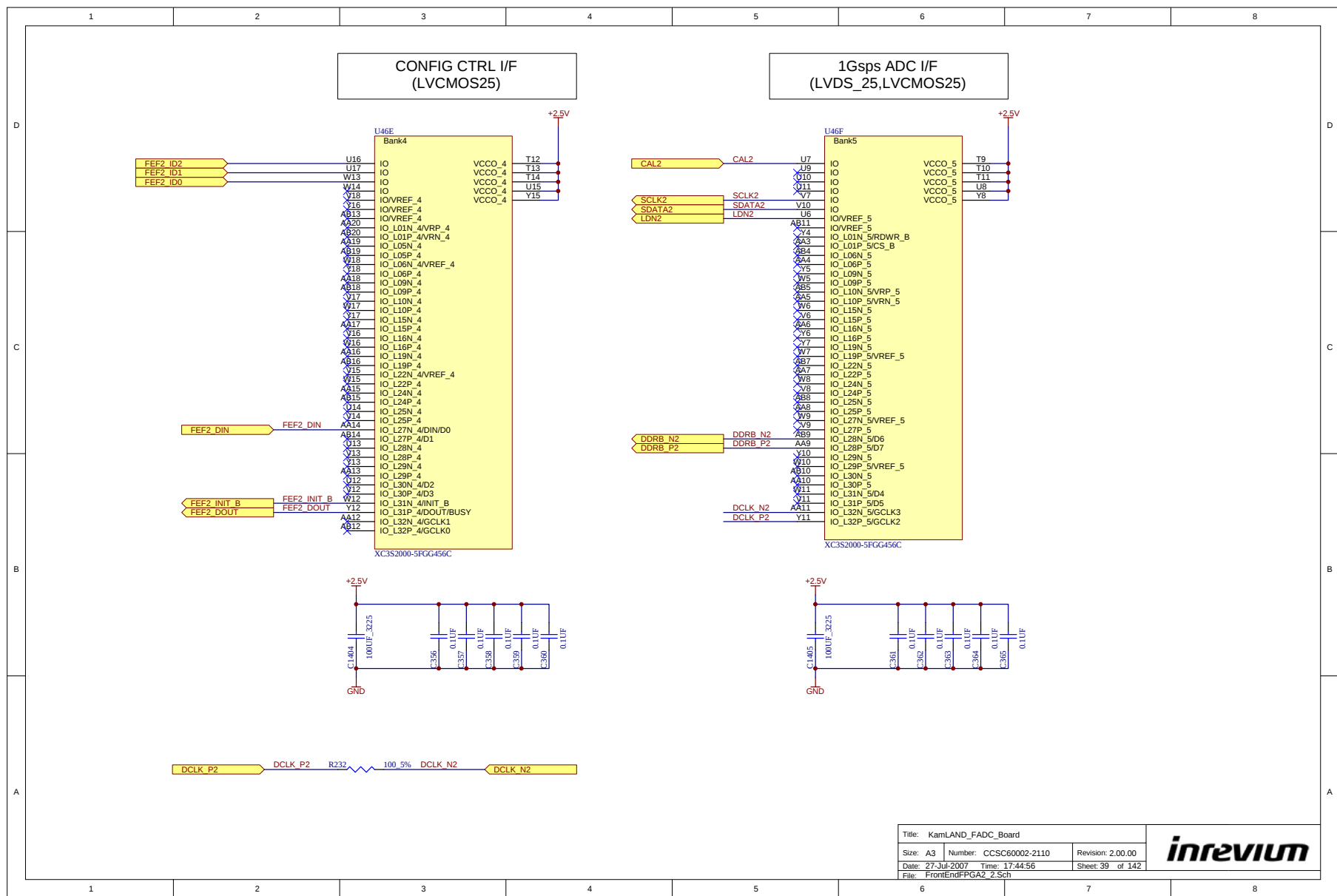


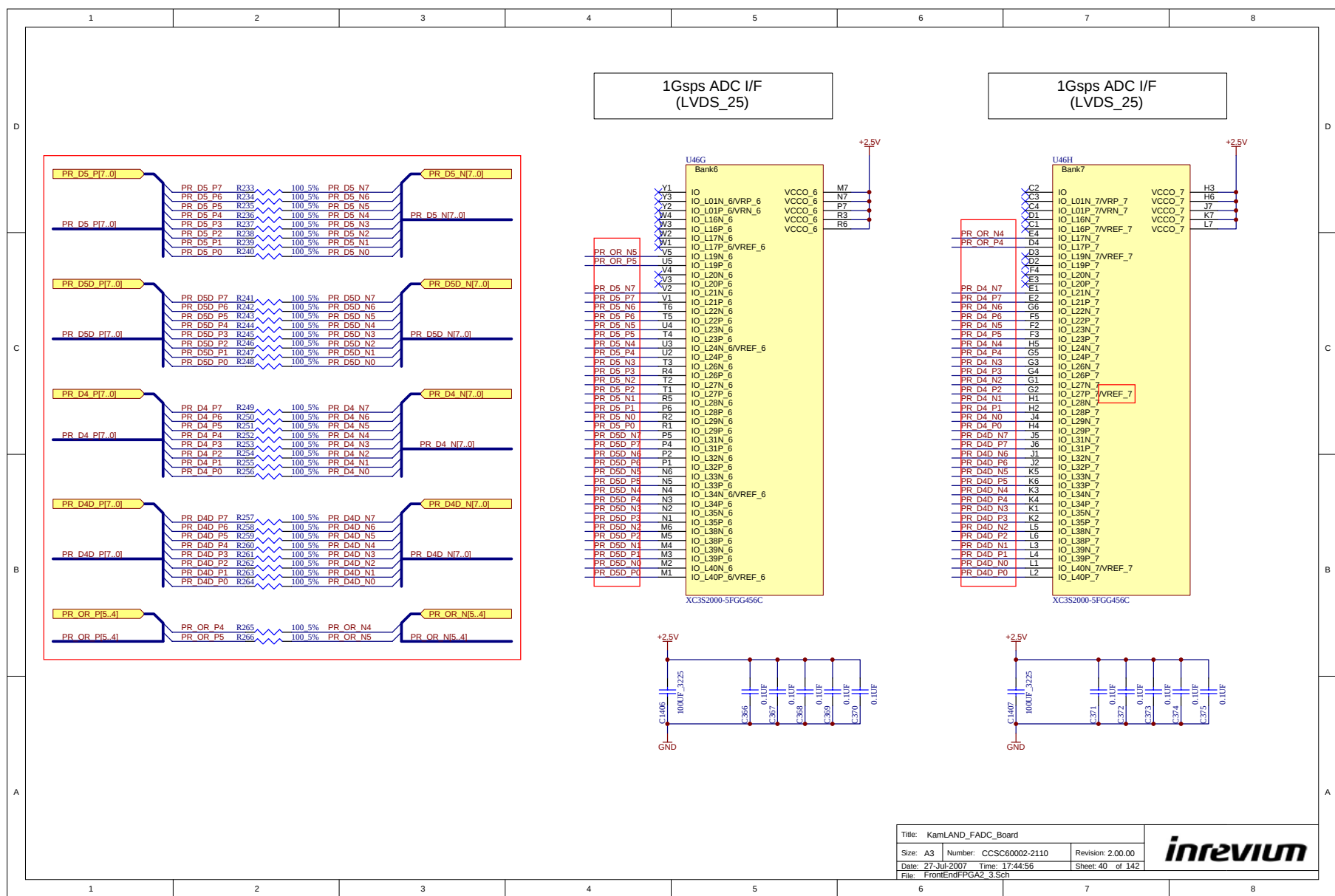
FrontEnd FPGA 2 TOP

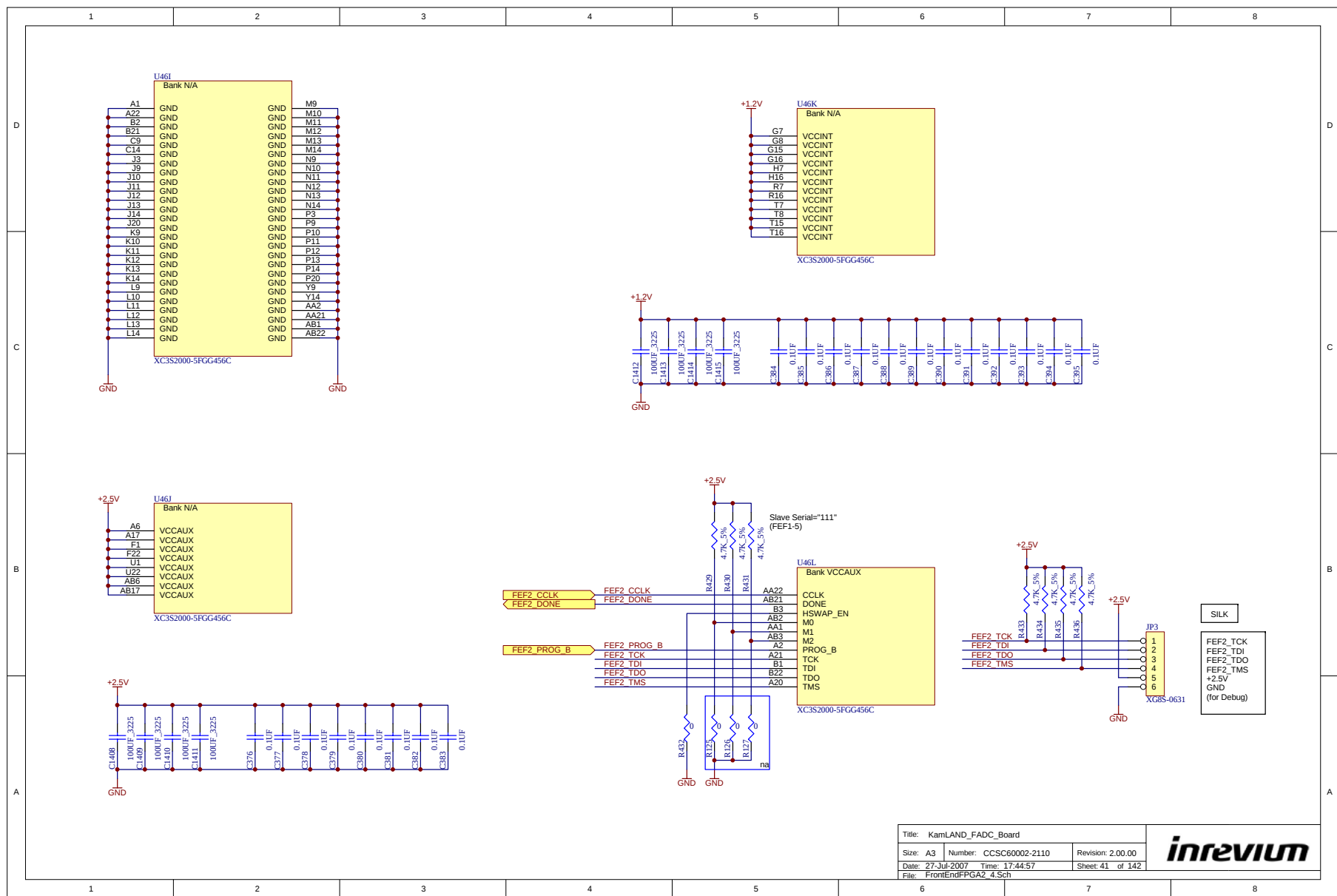




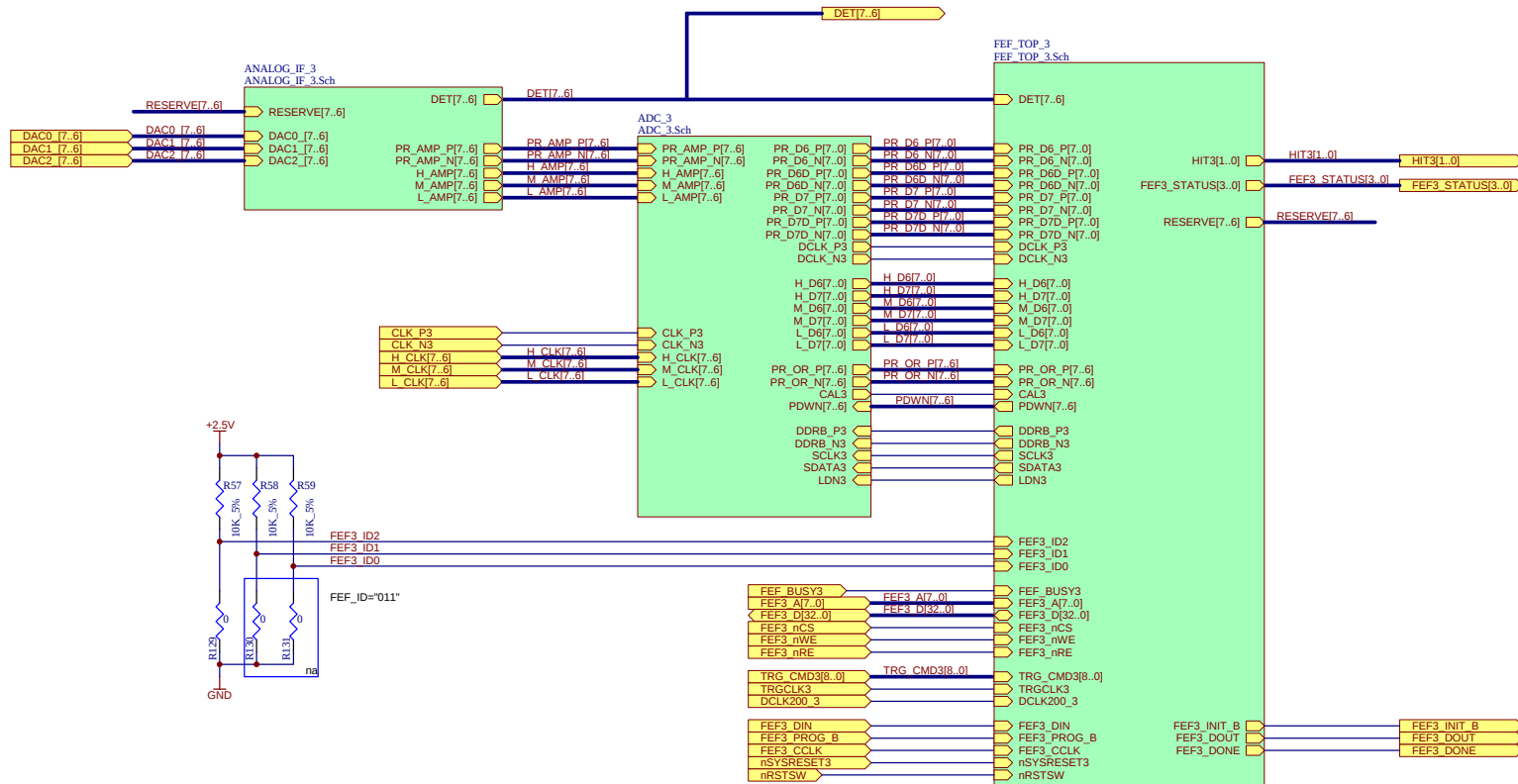


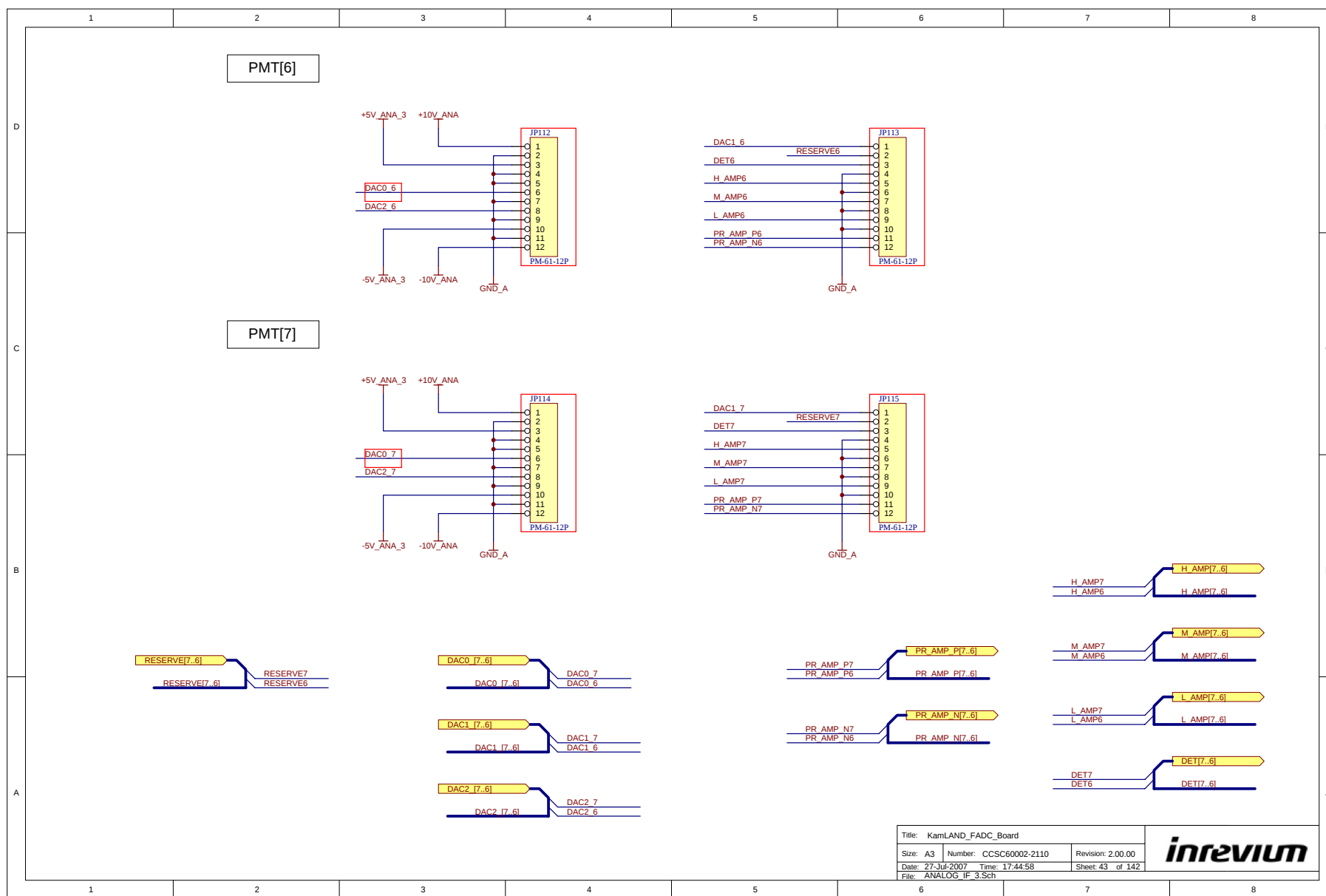




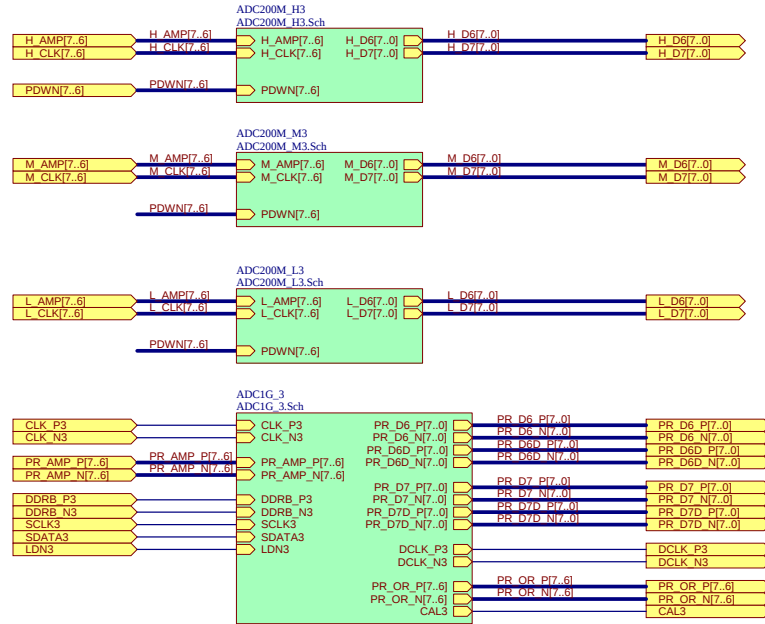


PMT[7..6] to FrontEnd FPGA 3 TOP



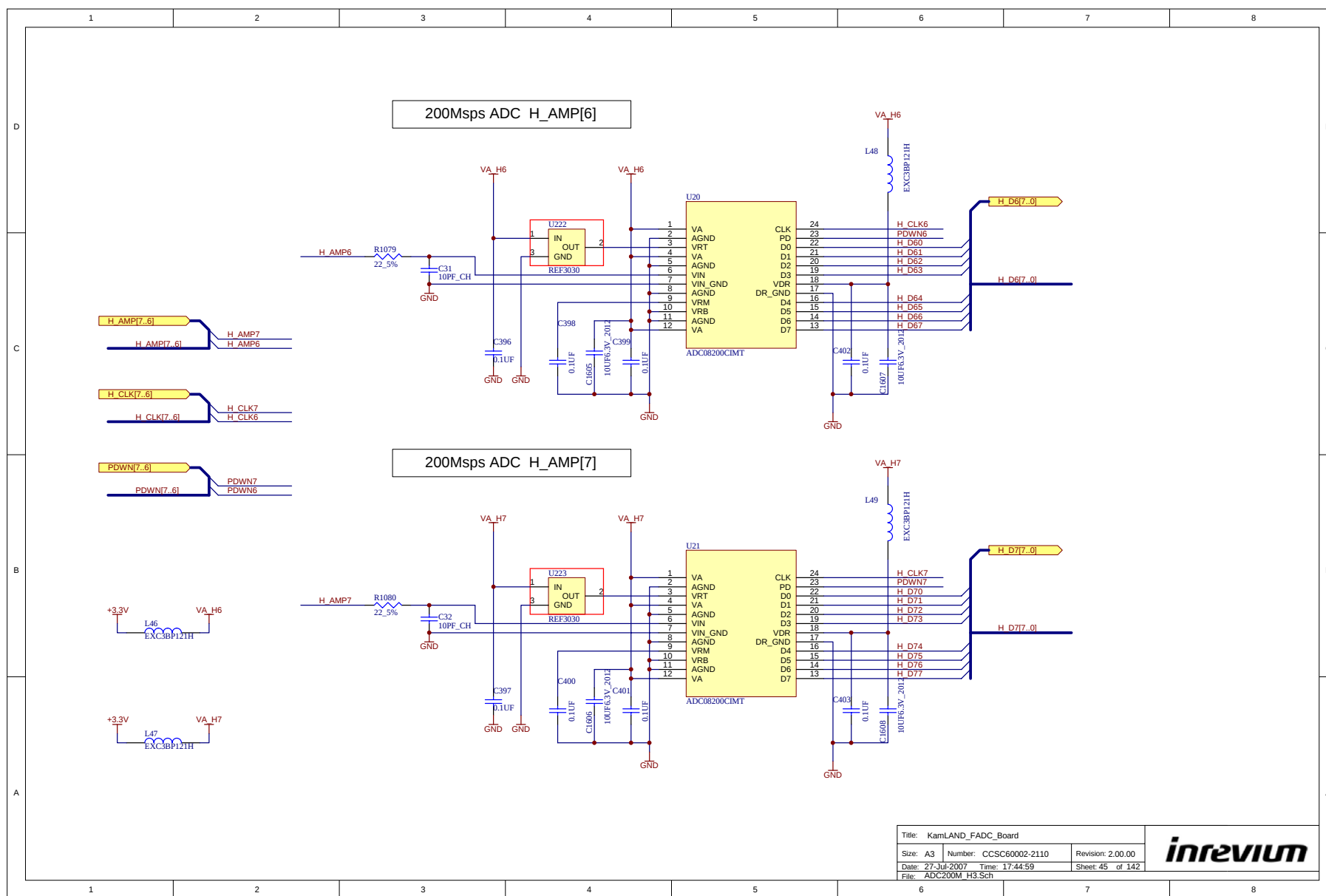


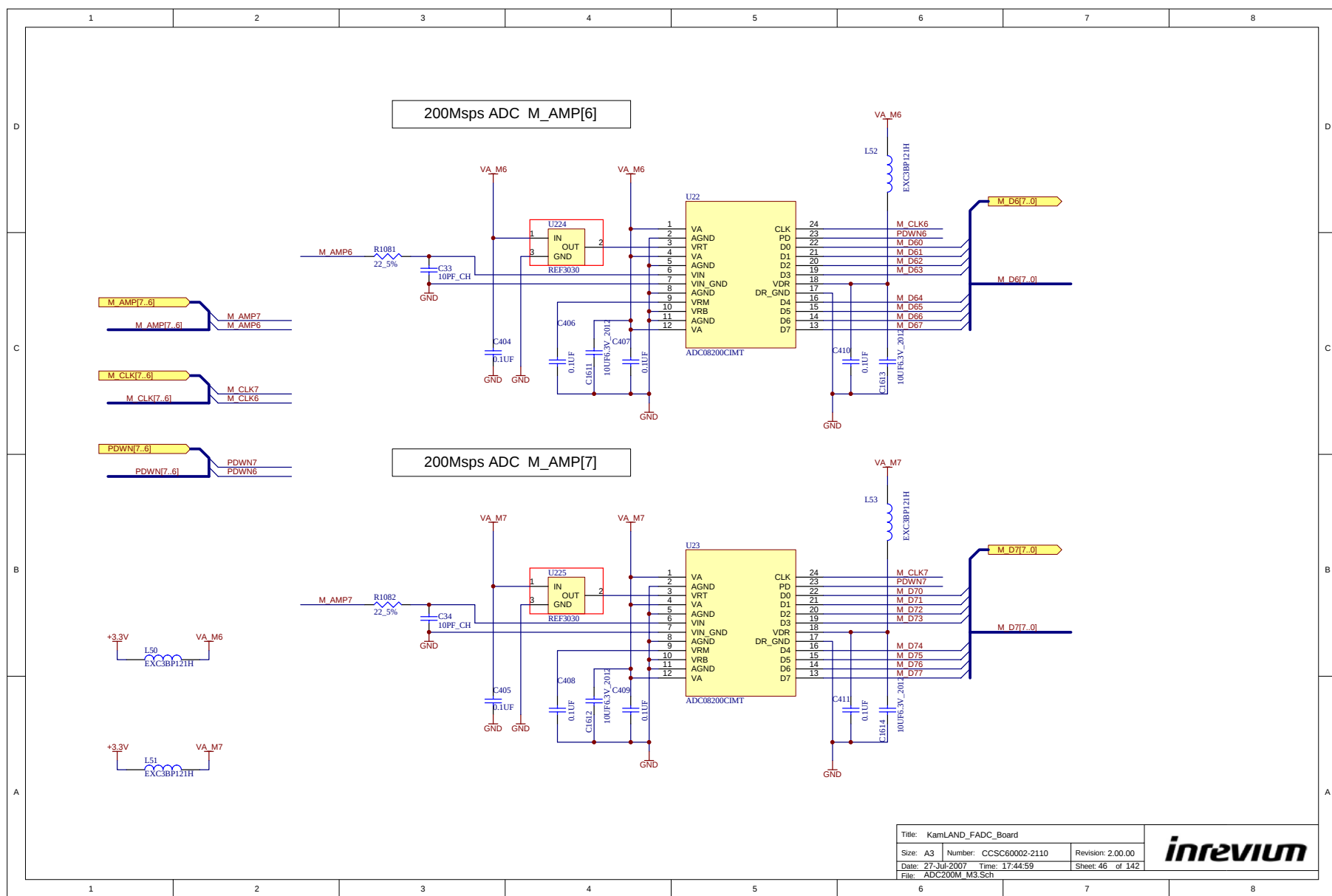
ADC[7..6]
TOP



Title: KamLAND_FADC_Board
Size: A3 Number: CCSC60002-2110 Revision: 2.00.00
Date: 27-Jul-2007 Time: 17:44:58 Sheet: 44 of 142
File: ADC_3.Sch

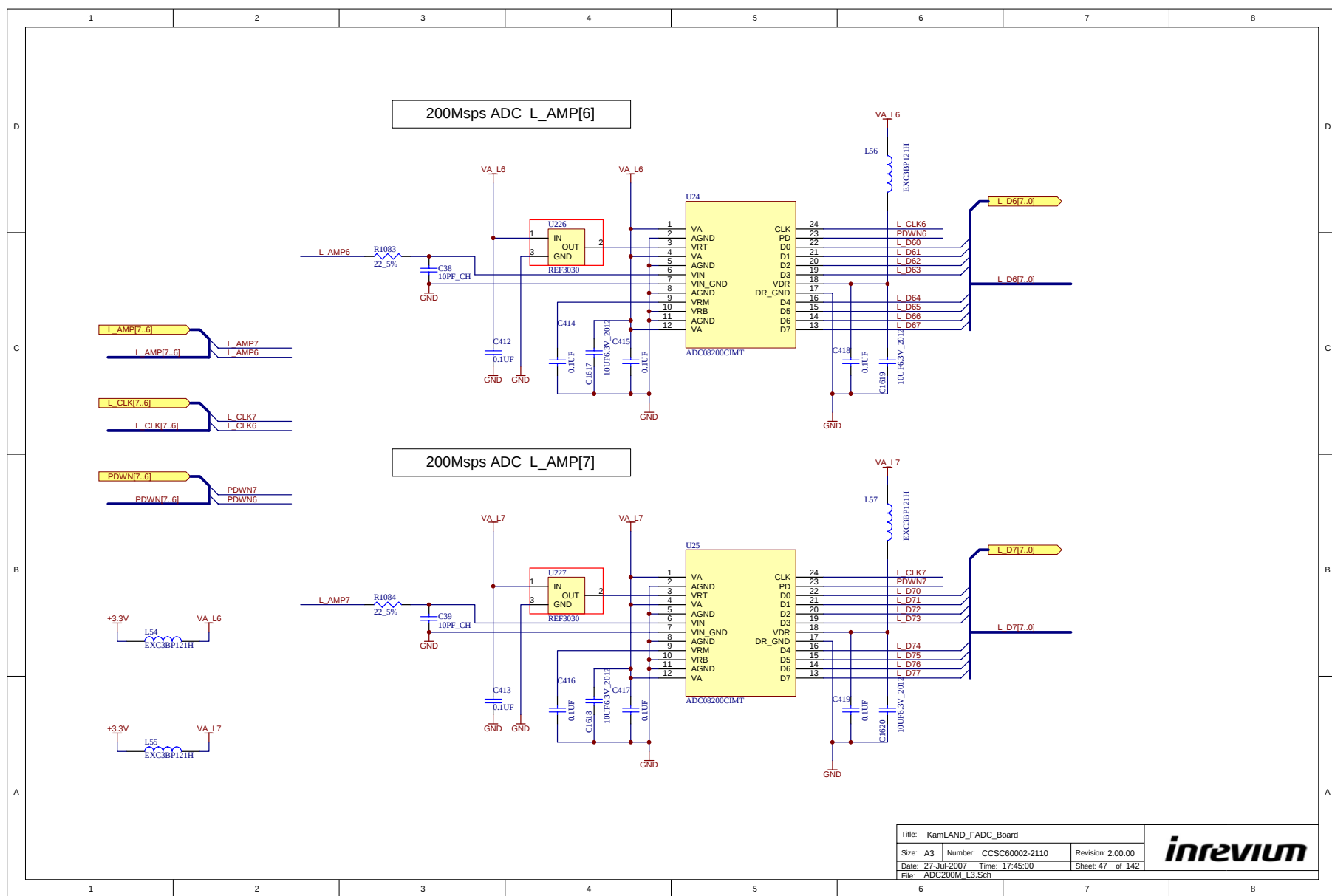
inrevium



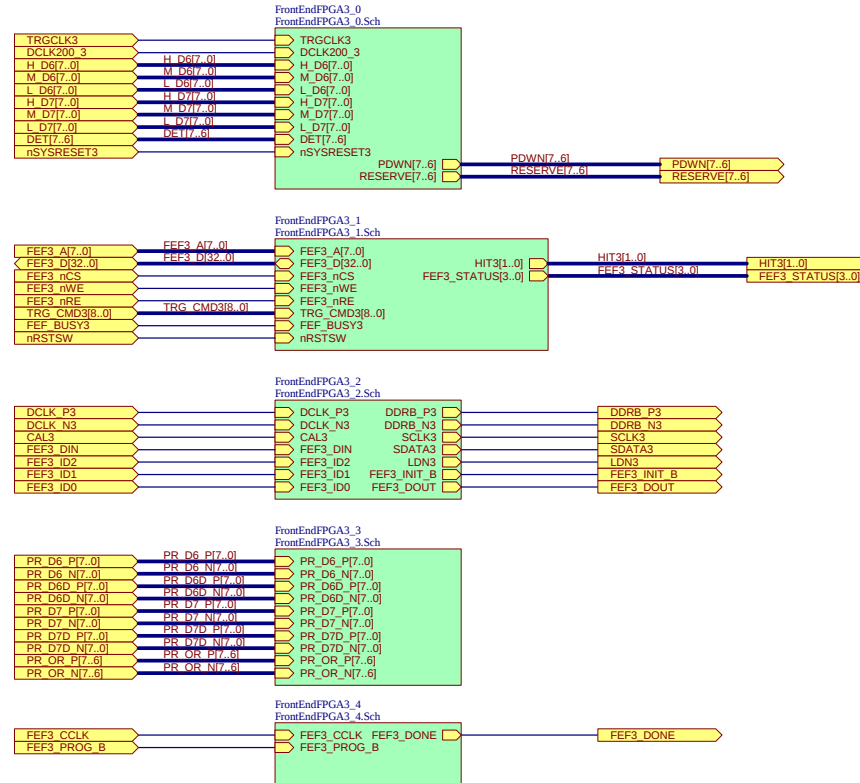


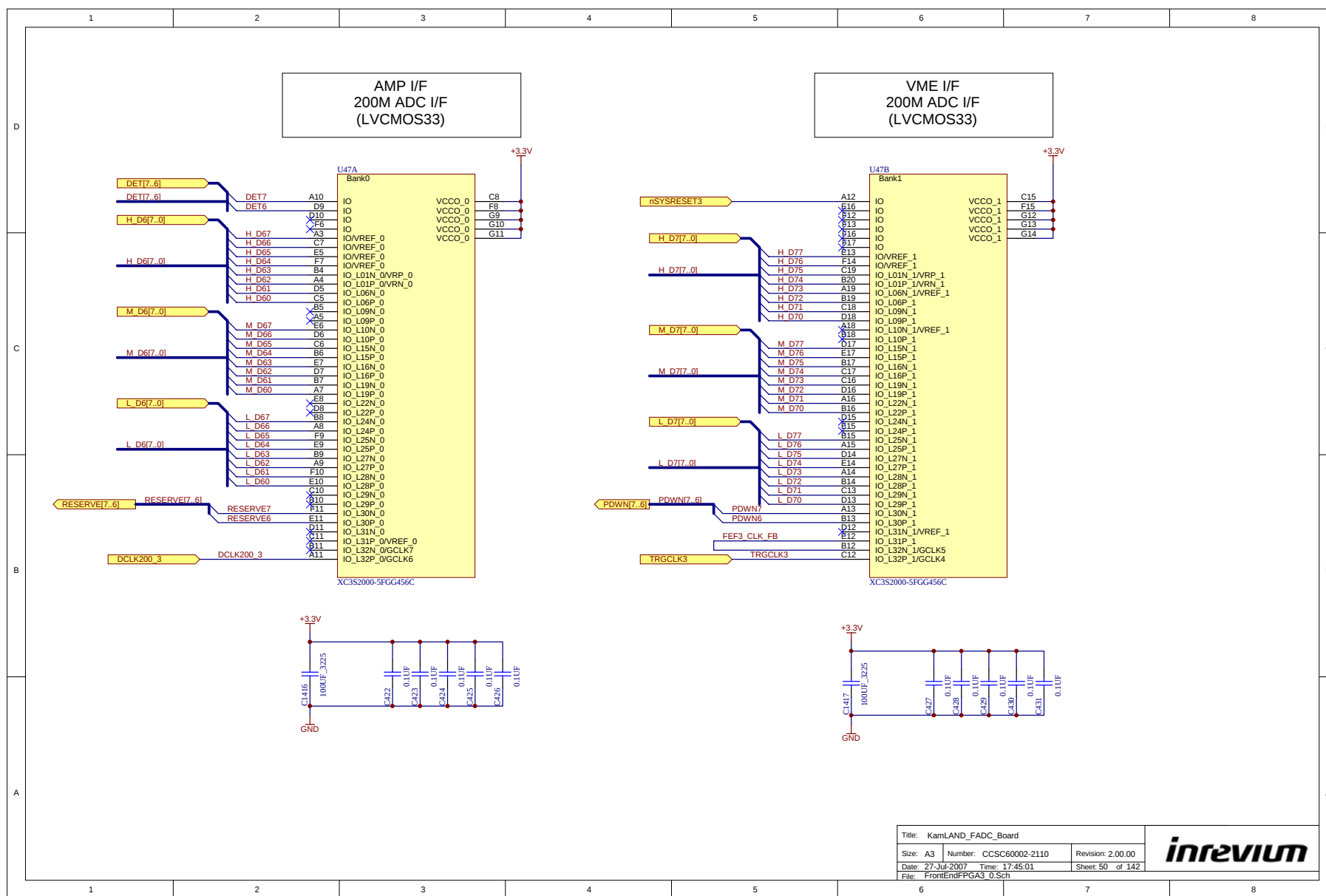
Title: KamLAND_FADC_Board	
Size: A3	Number: CCSC60002-2110
Date: 27-Jul-2007	Time: 17:44:59
File: ADC200M_M3.Sch	Revision: 2.00.00
	Sheet: 46 of 142

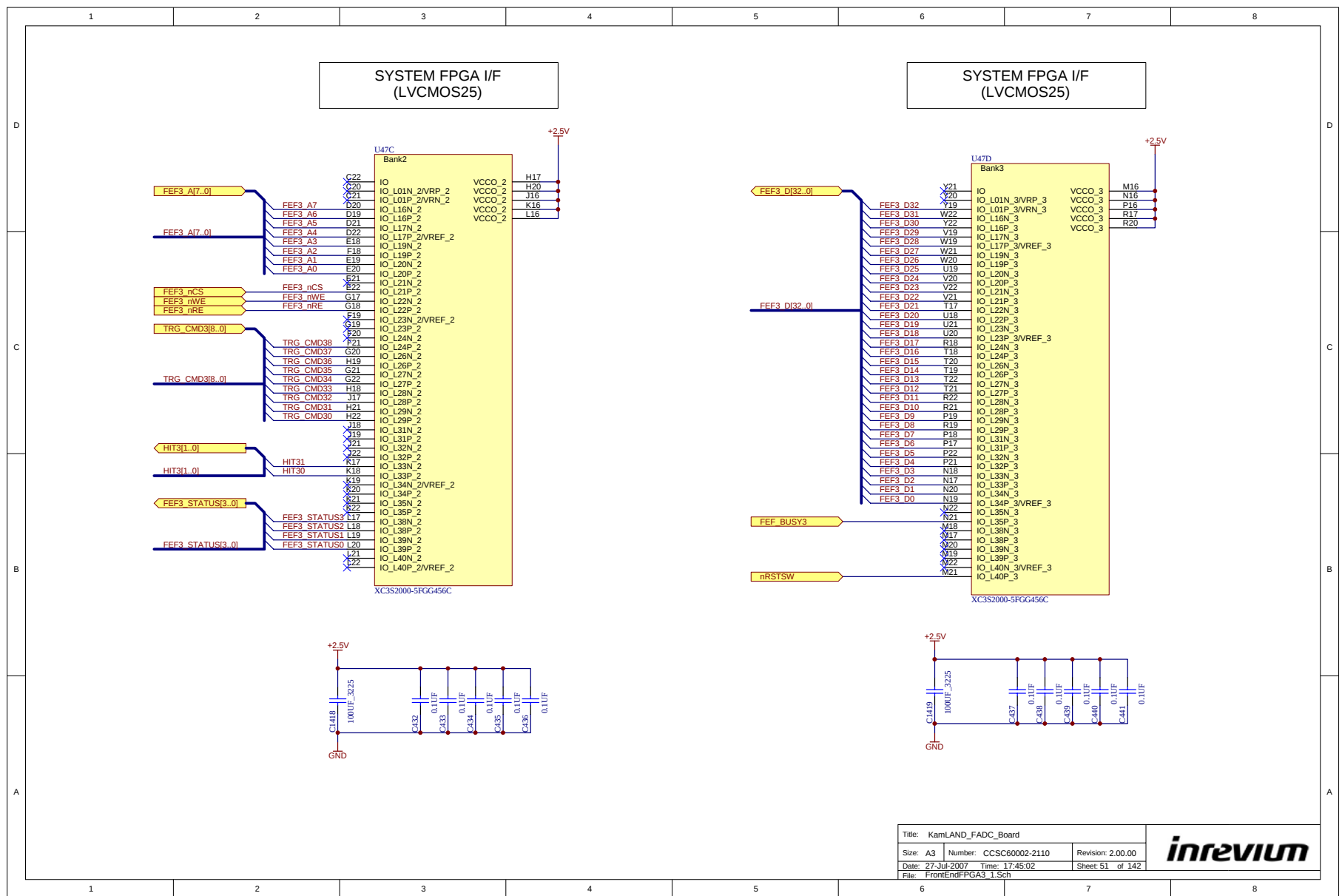
inrevium

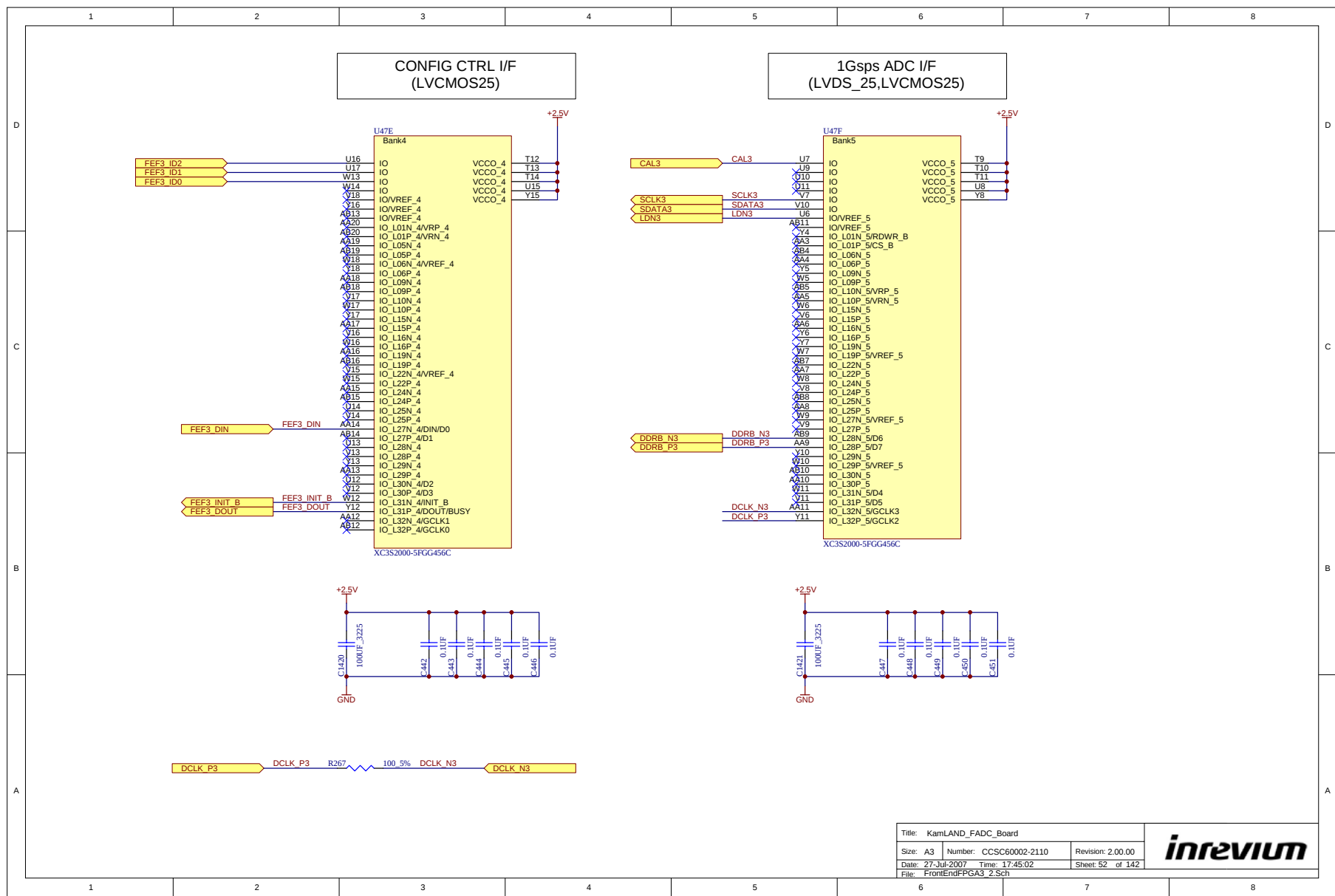


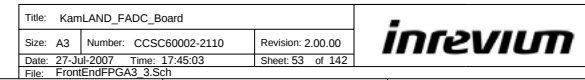
FrontEnd FPGA 3
TOP



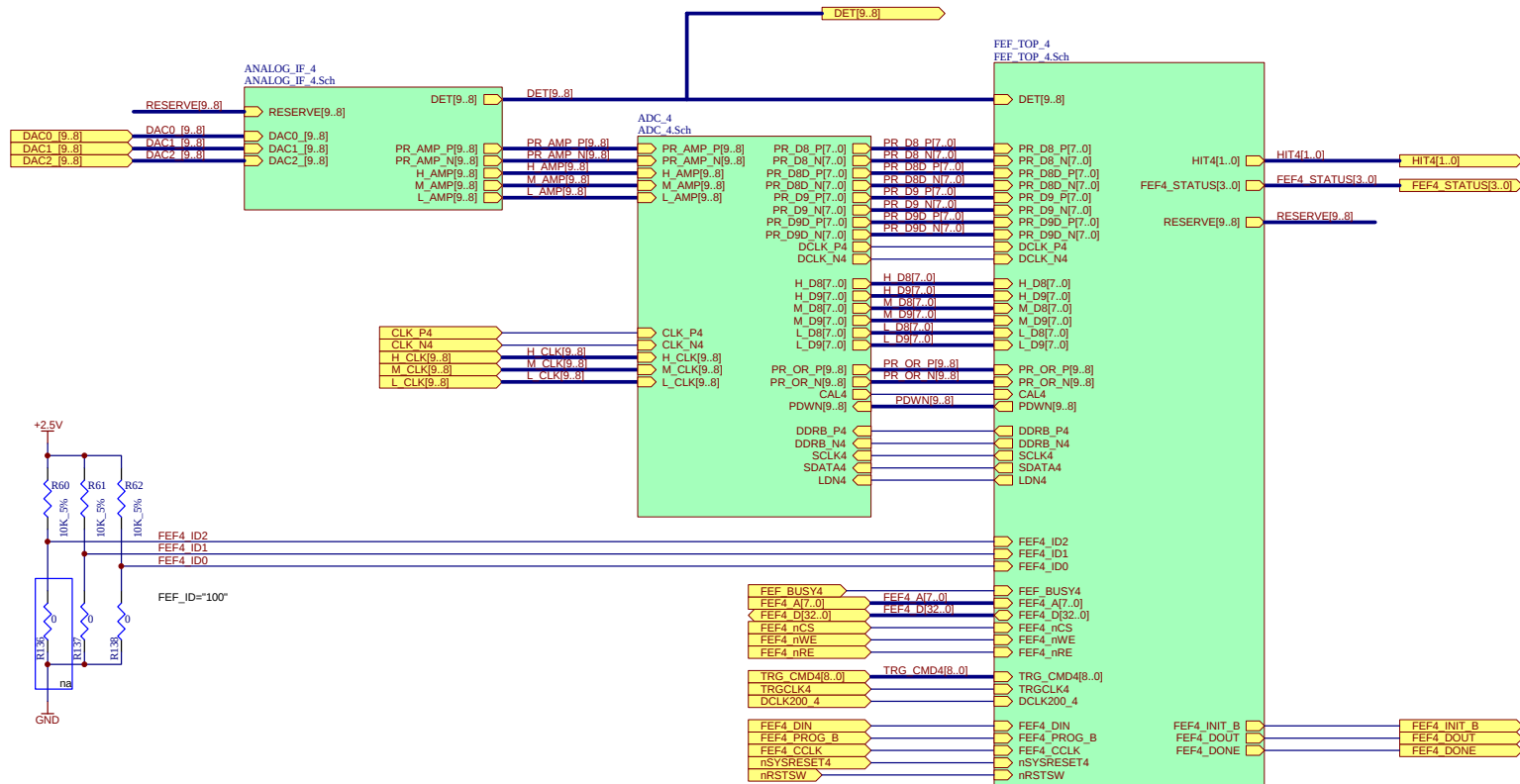


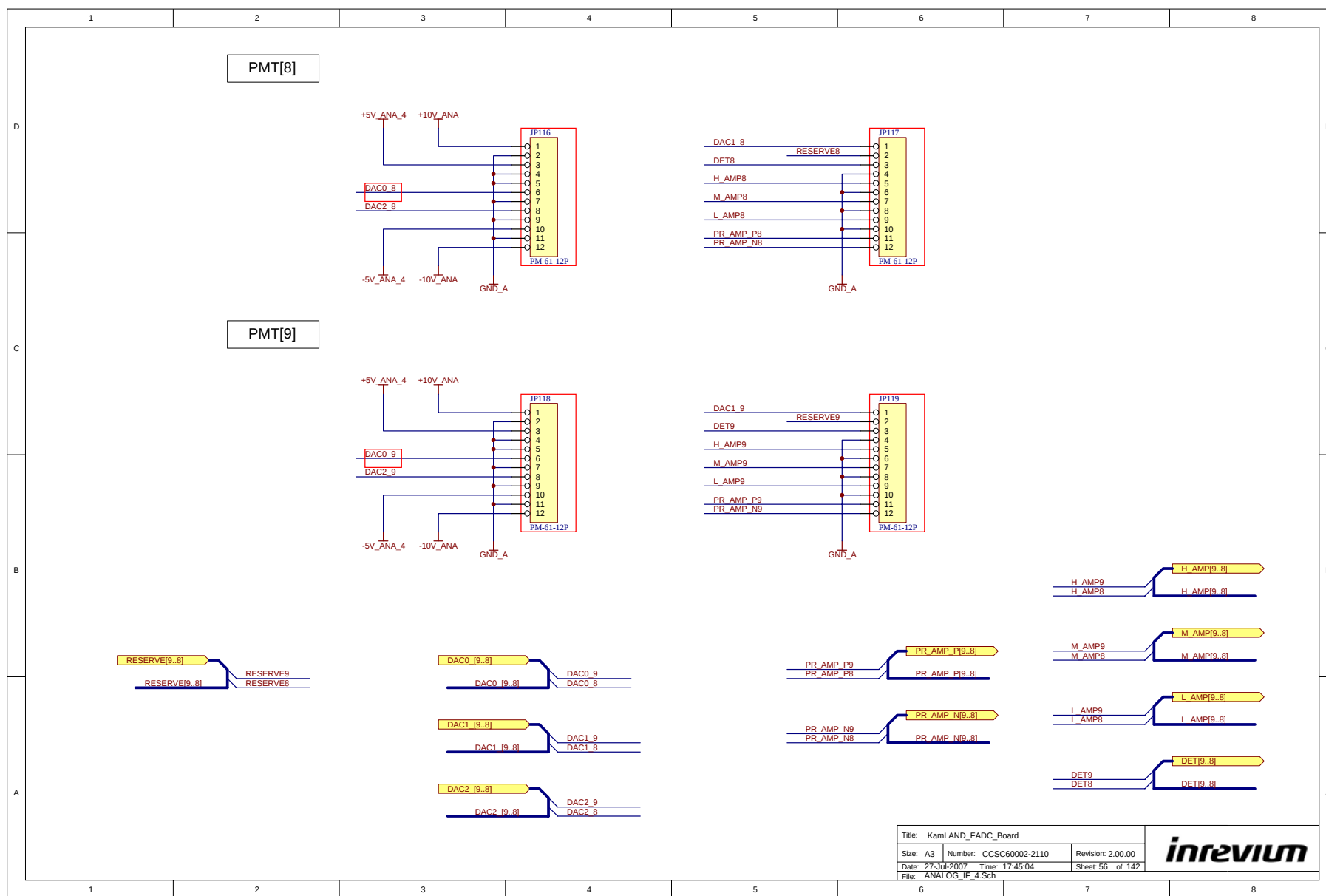




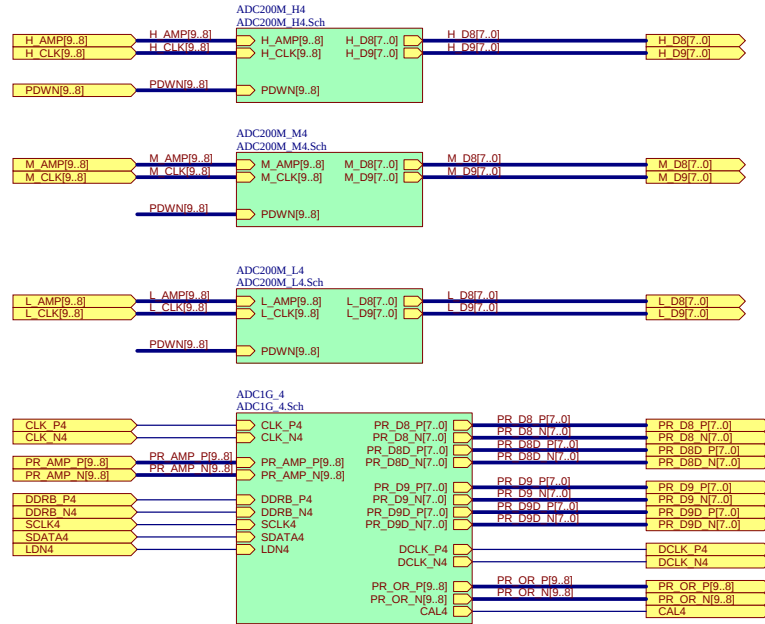


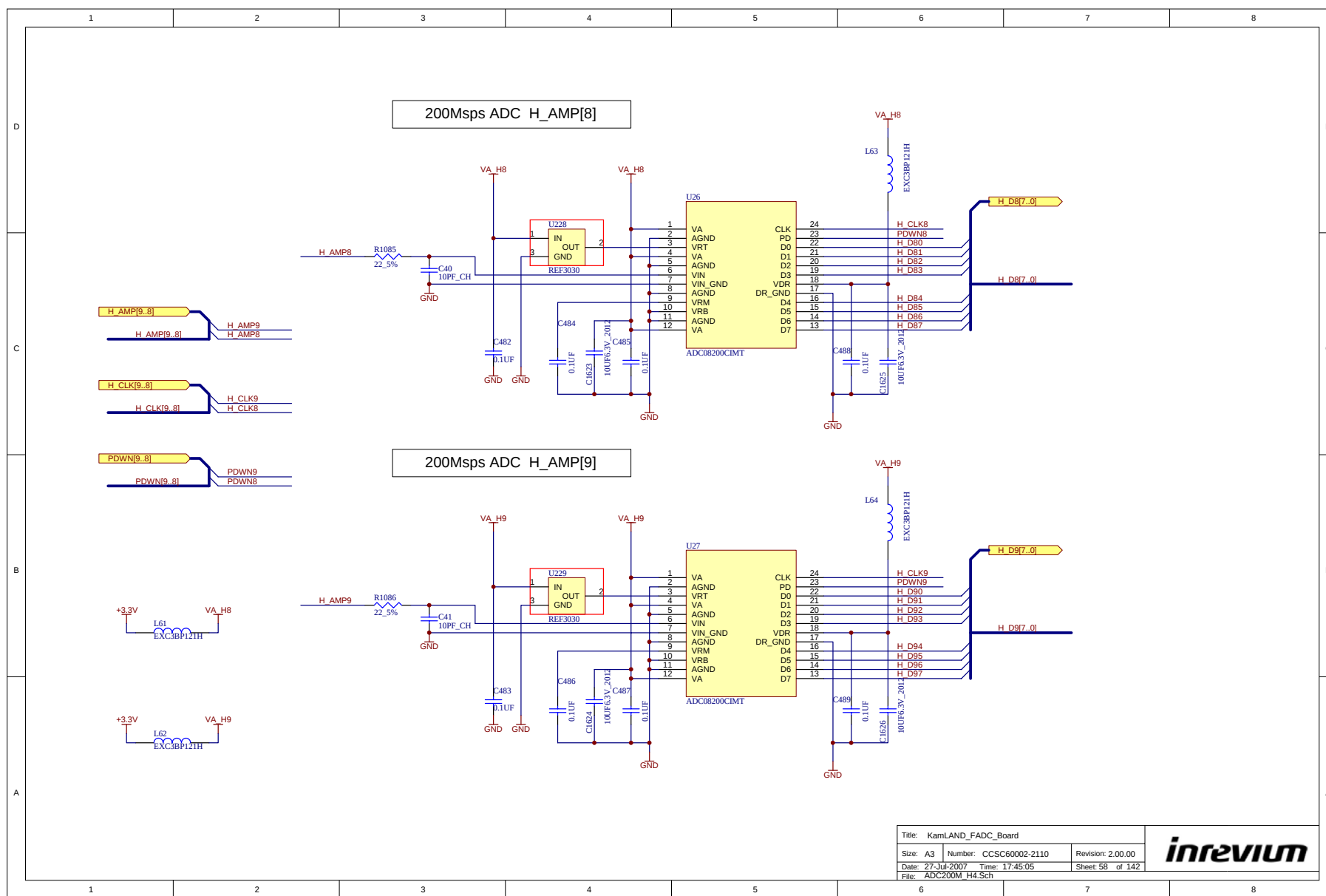
PMT[9..8] to FrontEnd FPGA 4 TOP





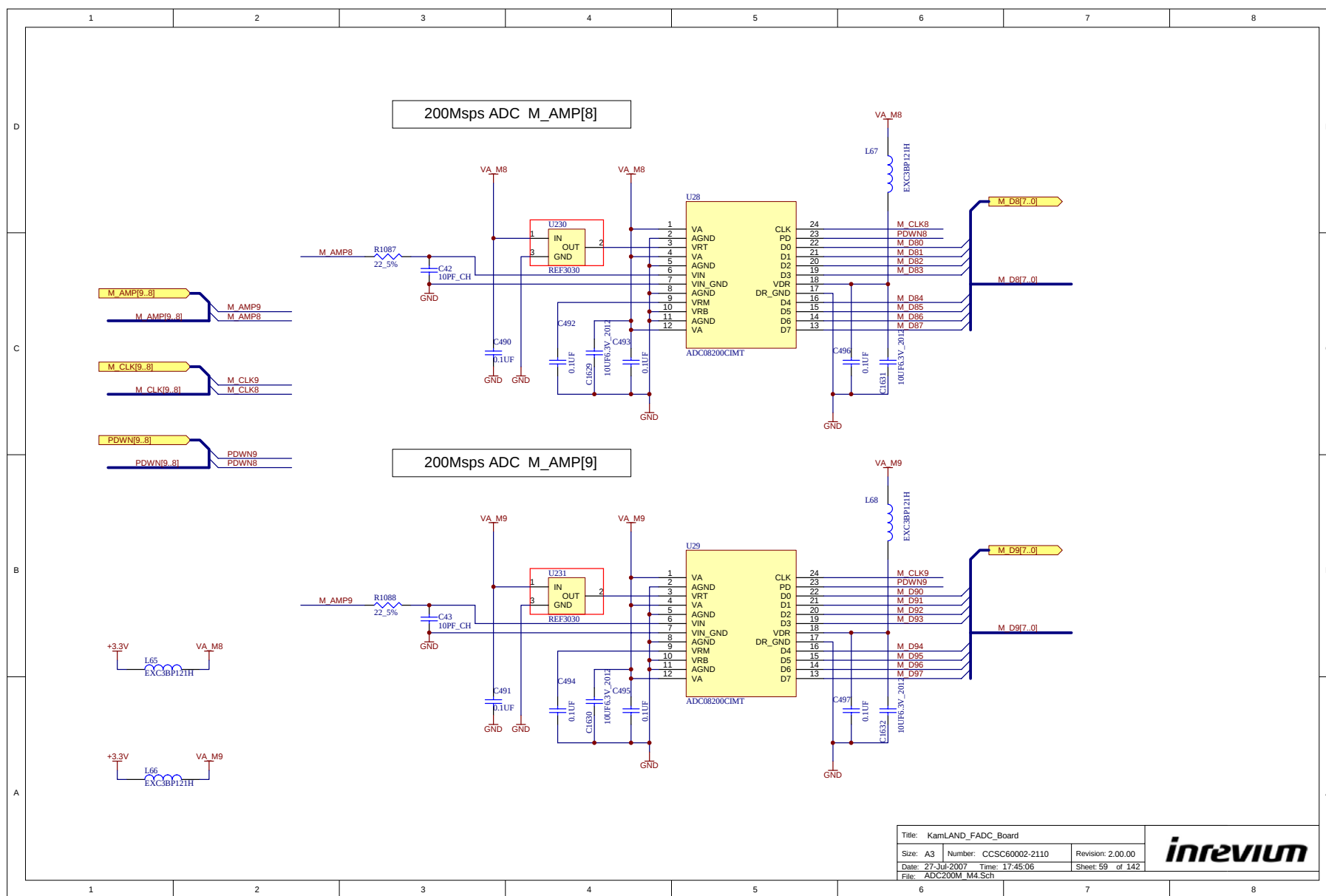
ADC[9..8]
TOP

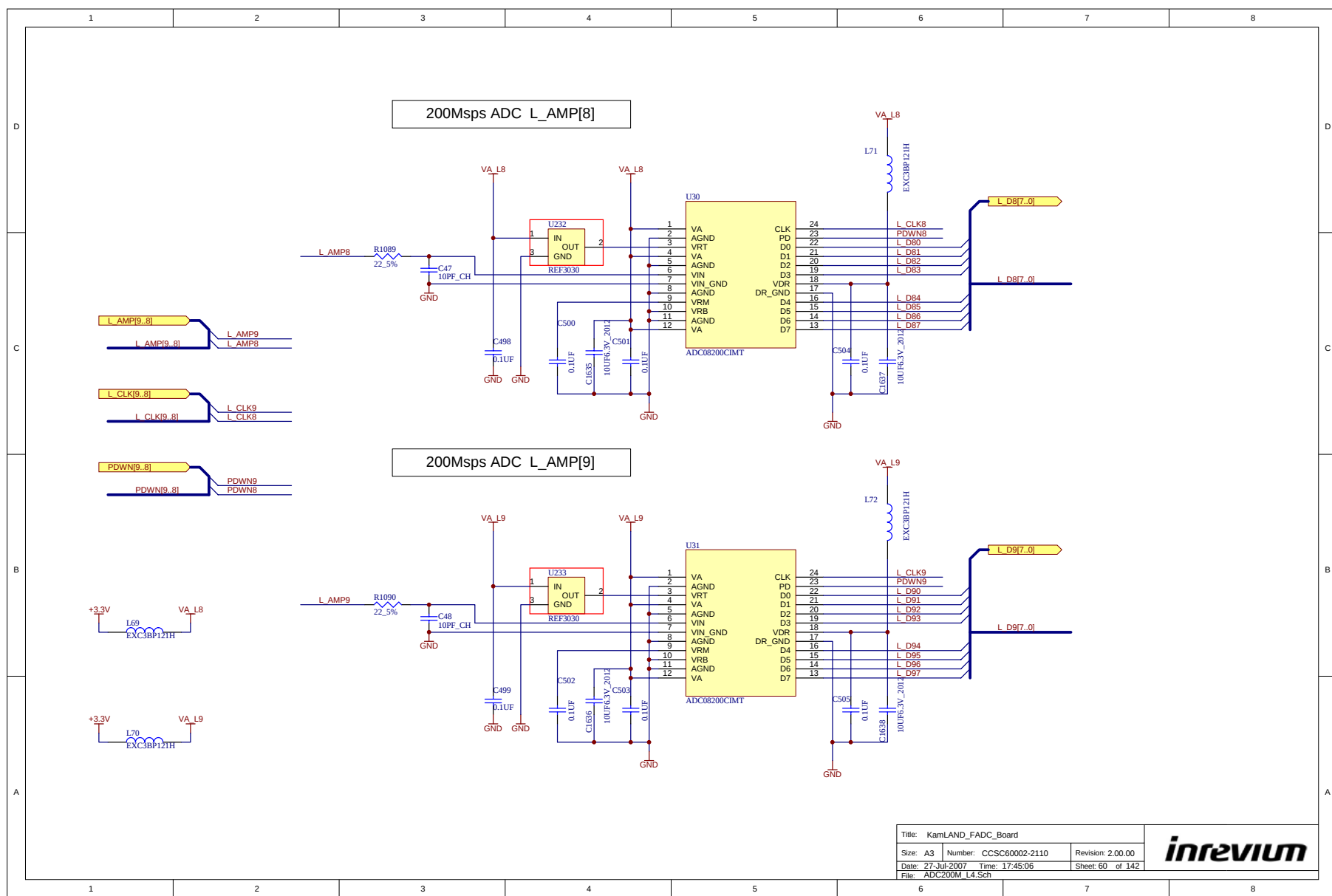




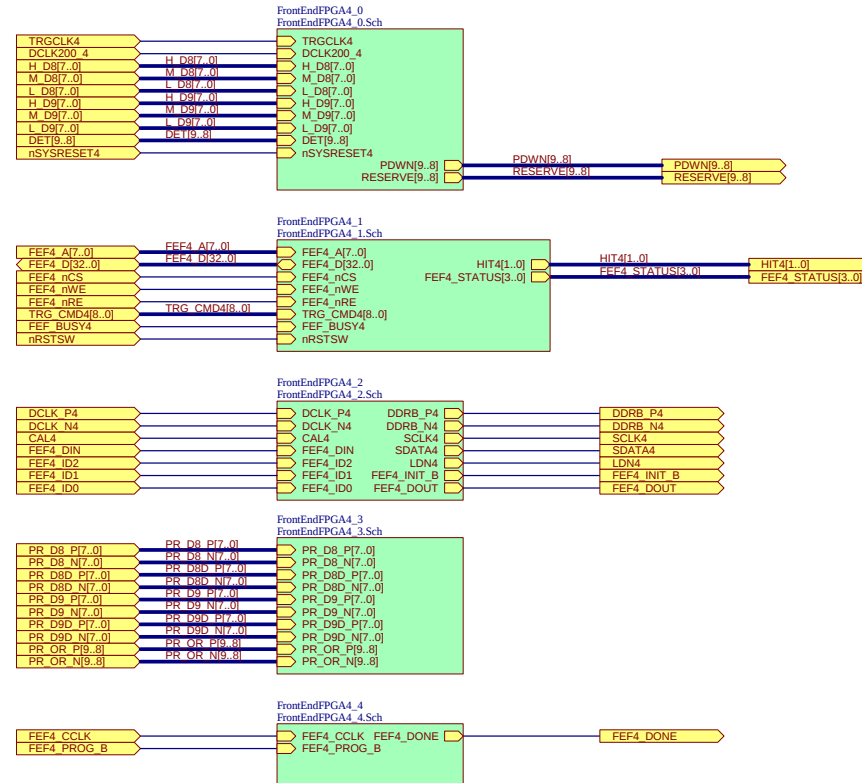
Title: KamLAND_FADC_Board	
Size: A3	Number: CCSC60002-2110
Date: 27-Jul-2007	Time: 17:45:05
File: ADC200M_H4.Sch	Revision: 2.00.00
	Sheet: 58 of 142

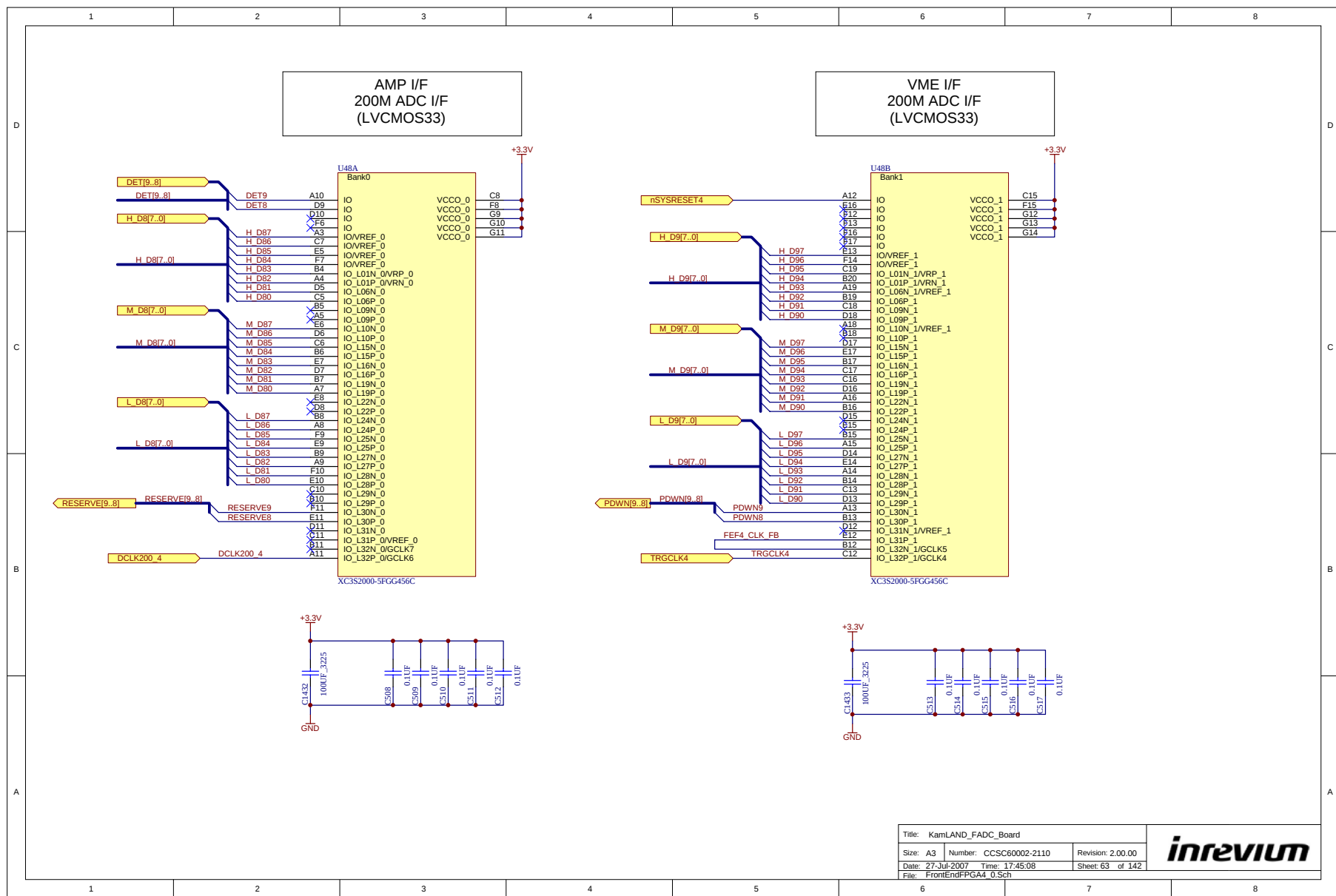
inrevium





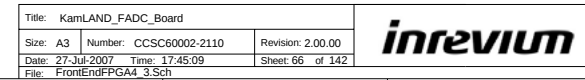
FrontEnd FPGA 4 TOP

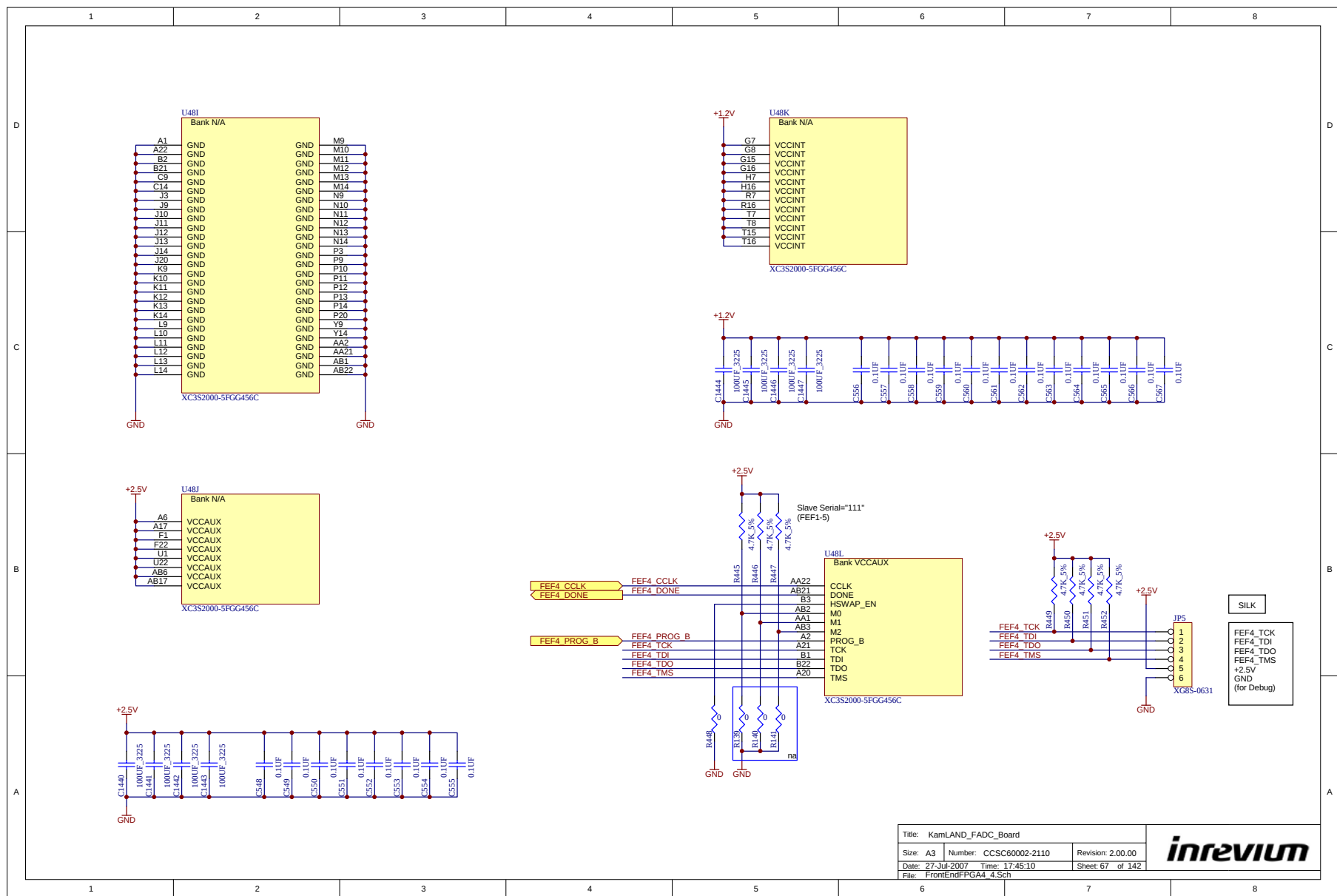




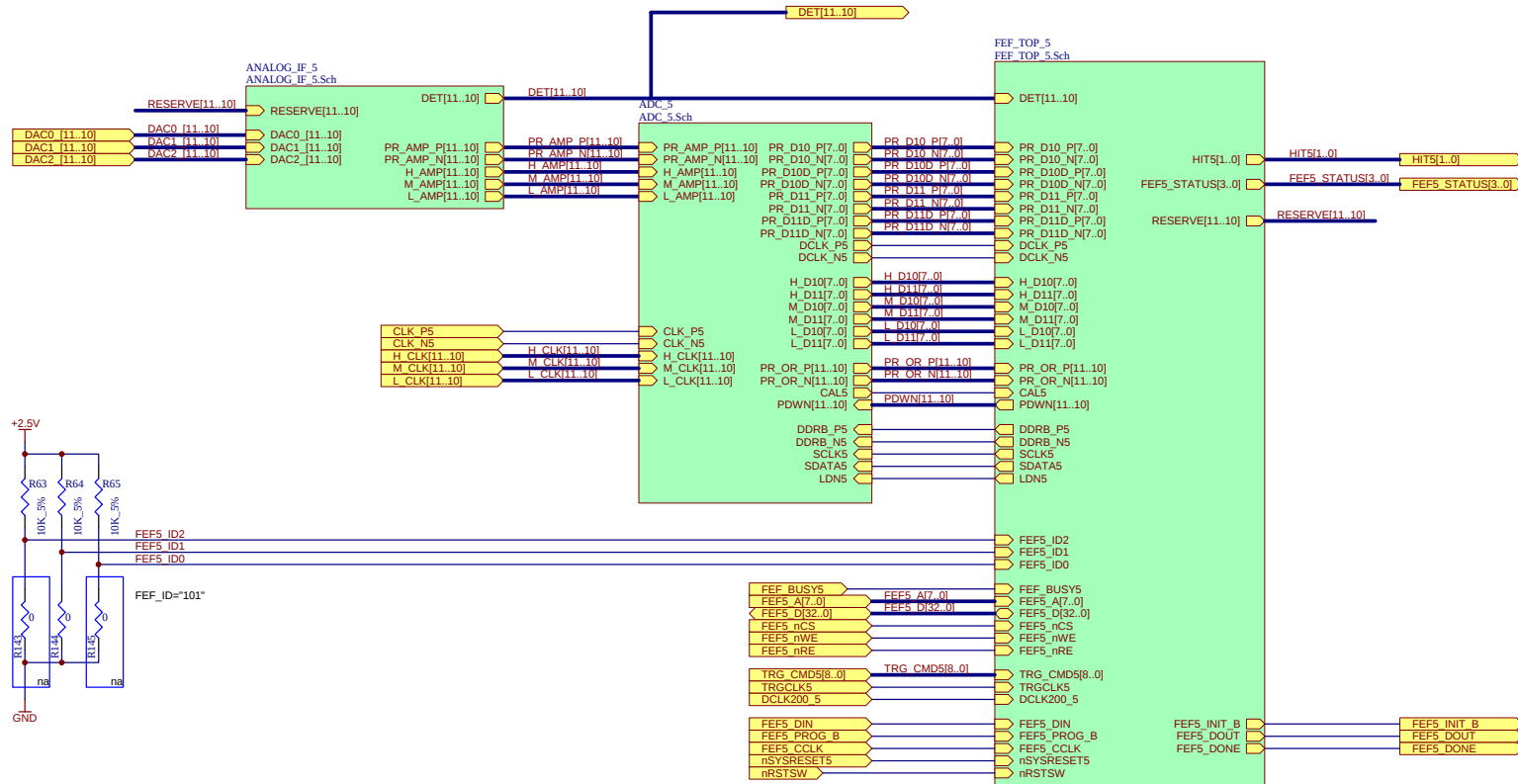
Title: KamLAND_FADC_Board		
Size: A3	Number: CCSC60002-2110	Revision: 2.00.00
Date: 27-Jul-2007	Time: 17:45:08	Sheet: 63 of 142
File: FrontEndFPGA4_0.Sch		

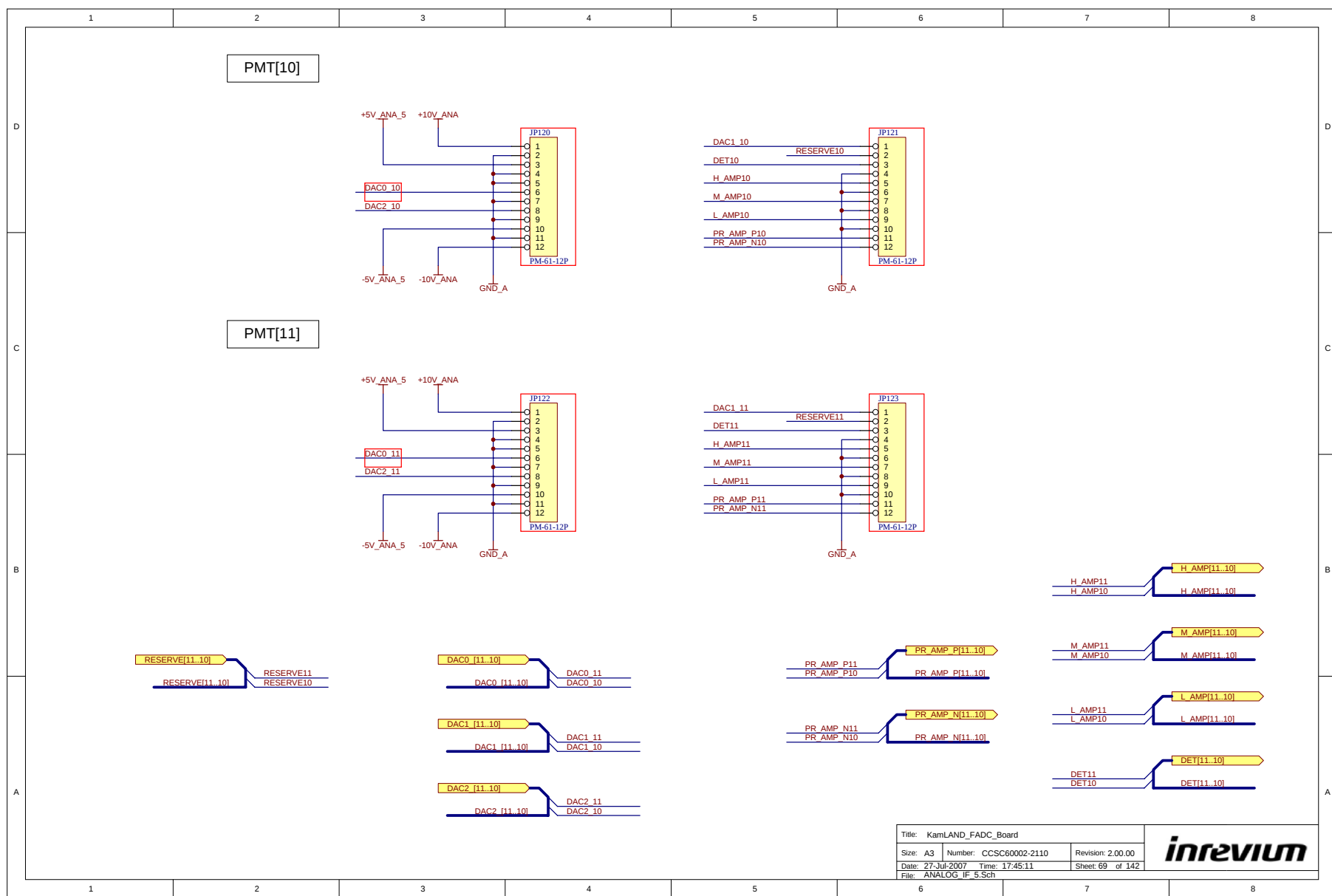




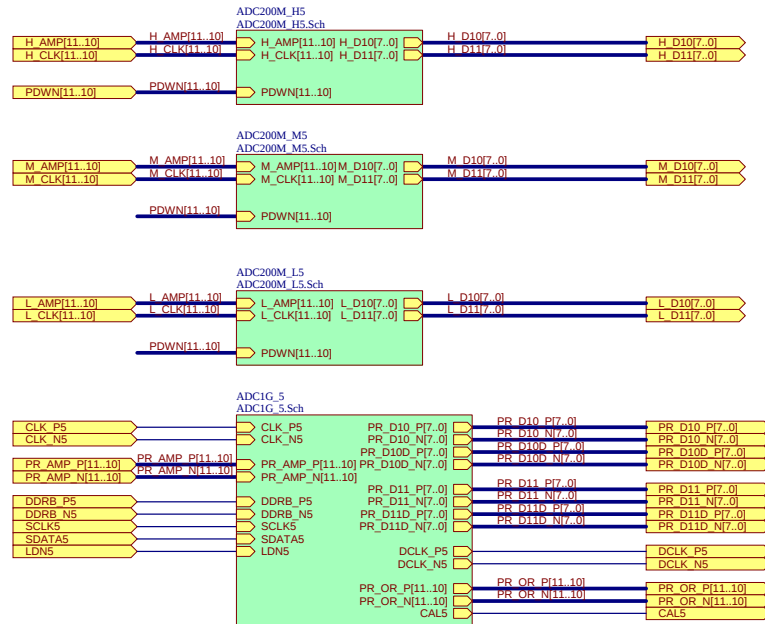


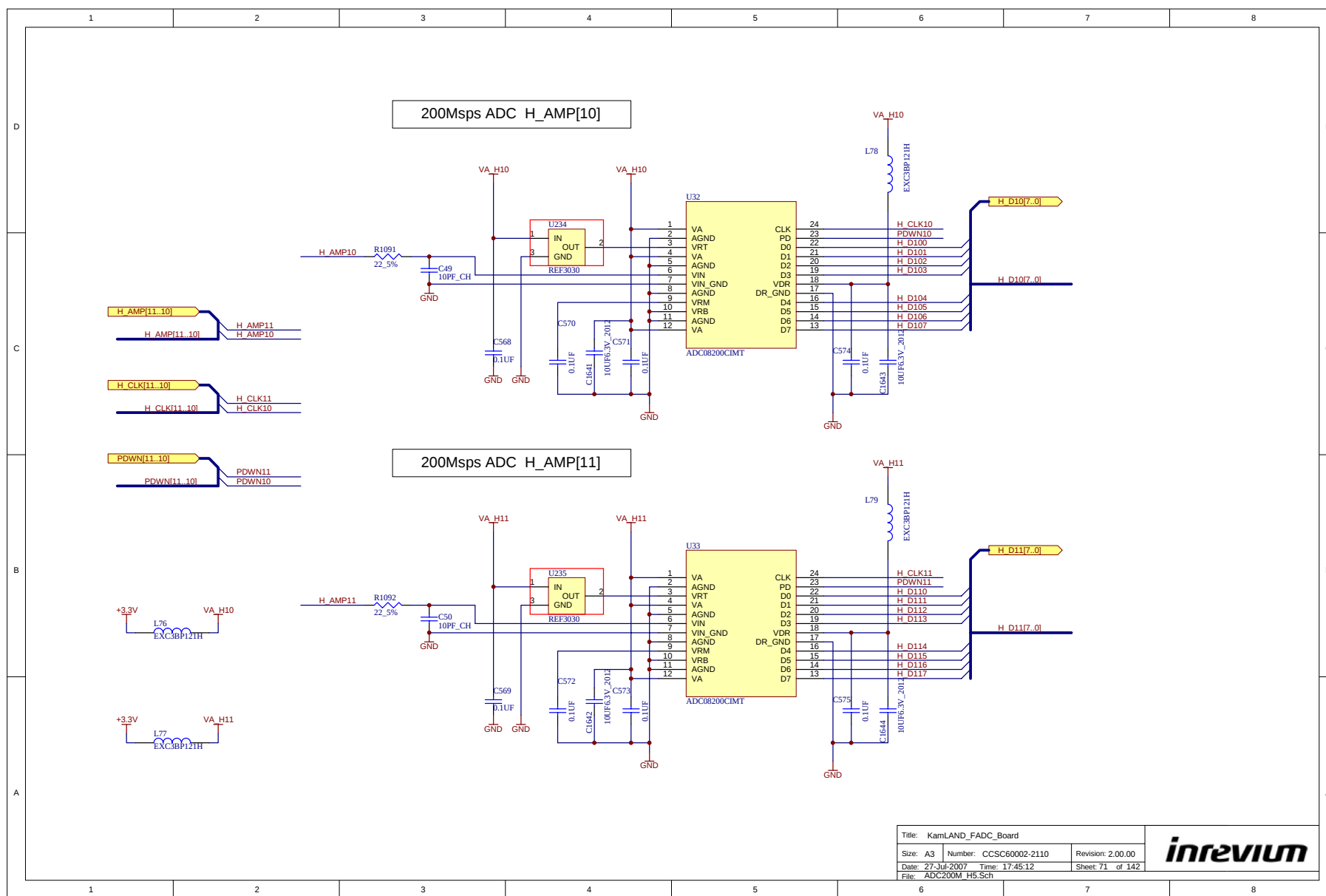
PMT[11..10] to FrontEnd FPGA 5 TOP

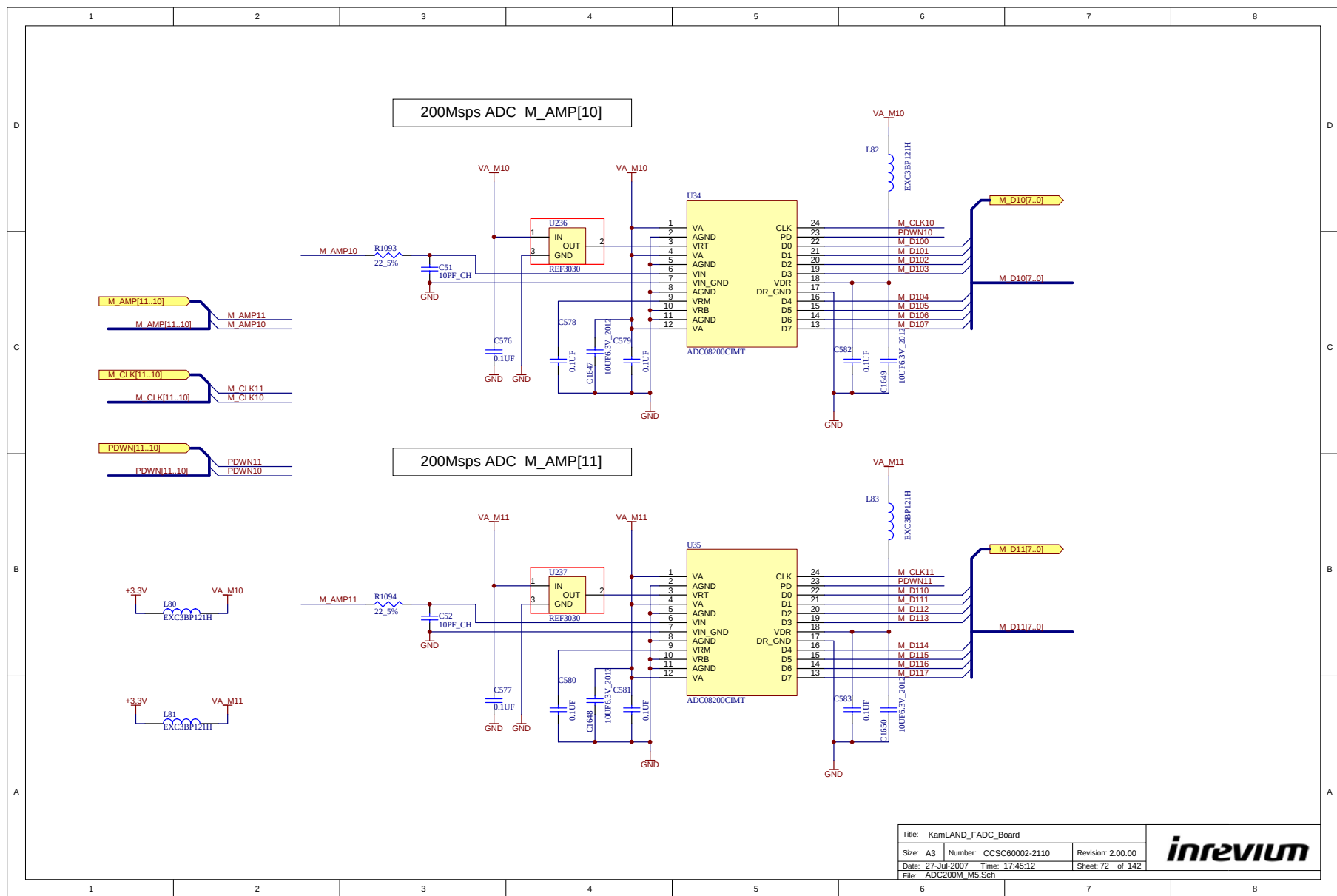


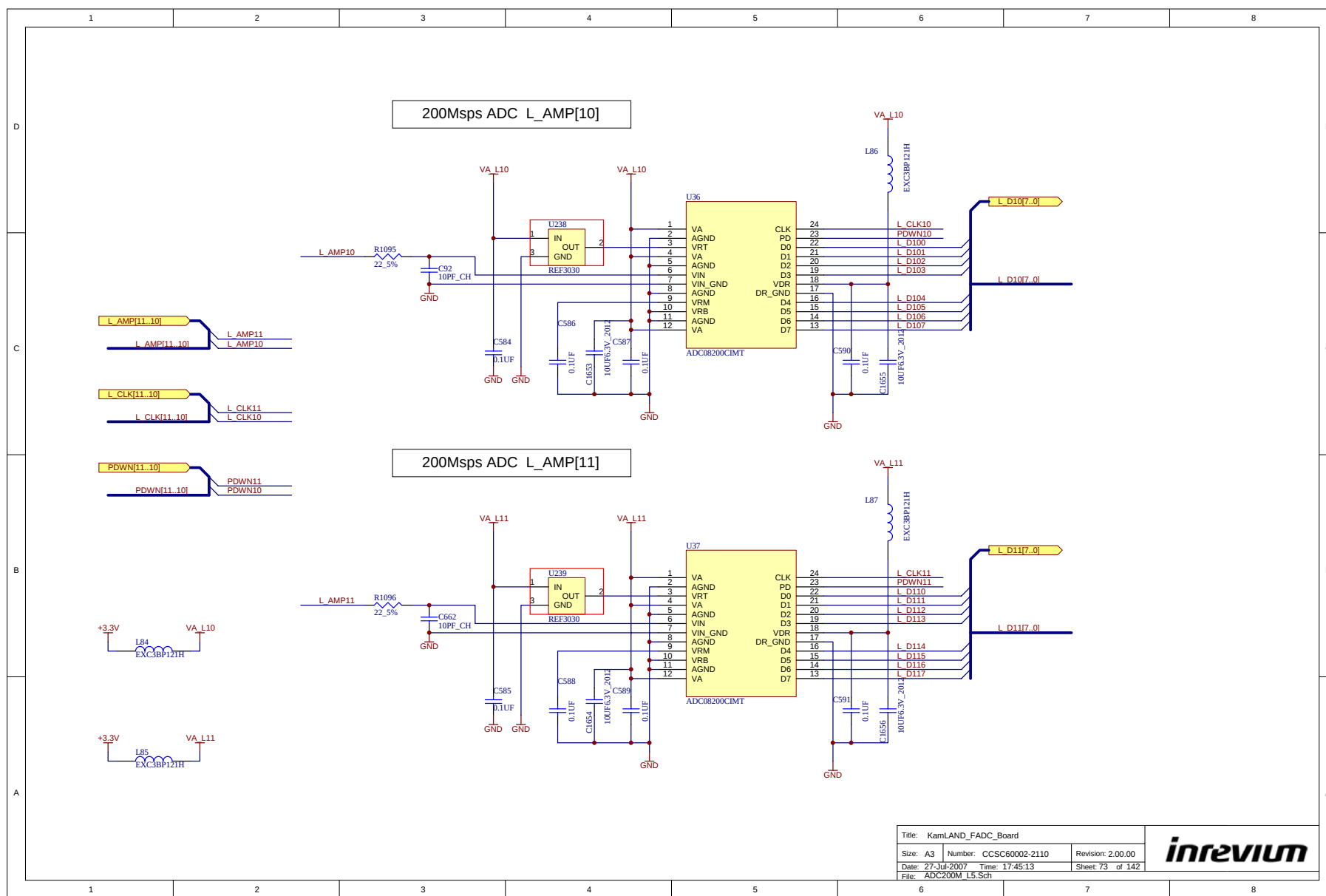


ADC[11..10]
TOP

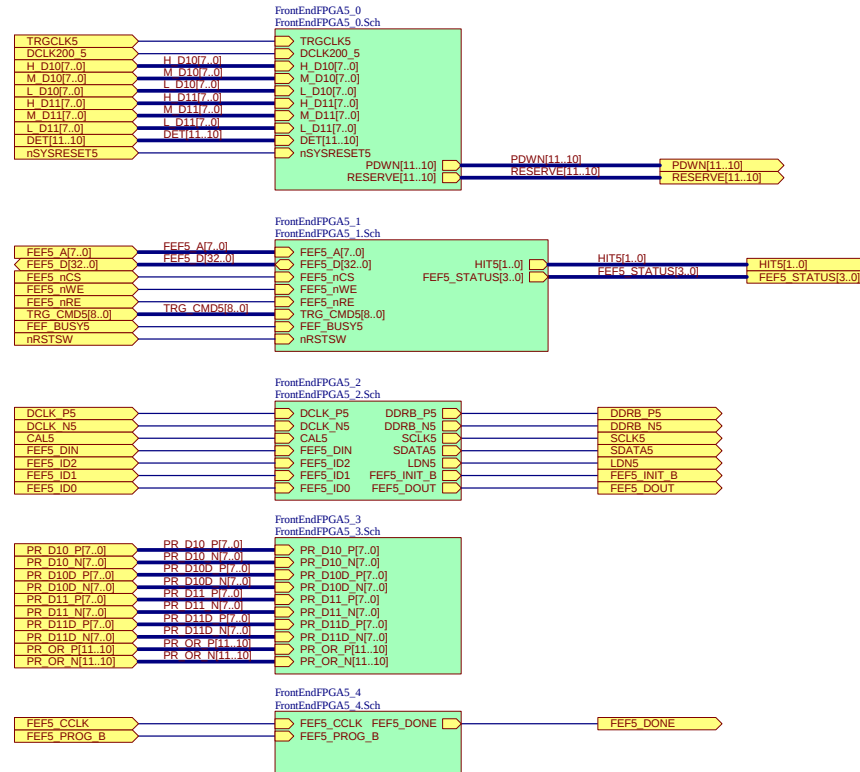


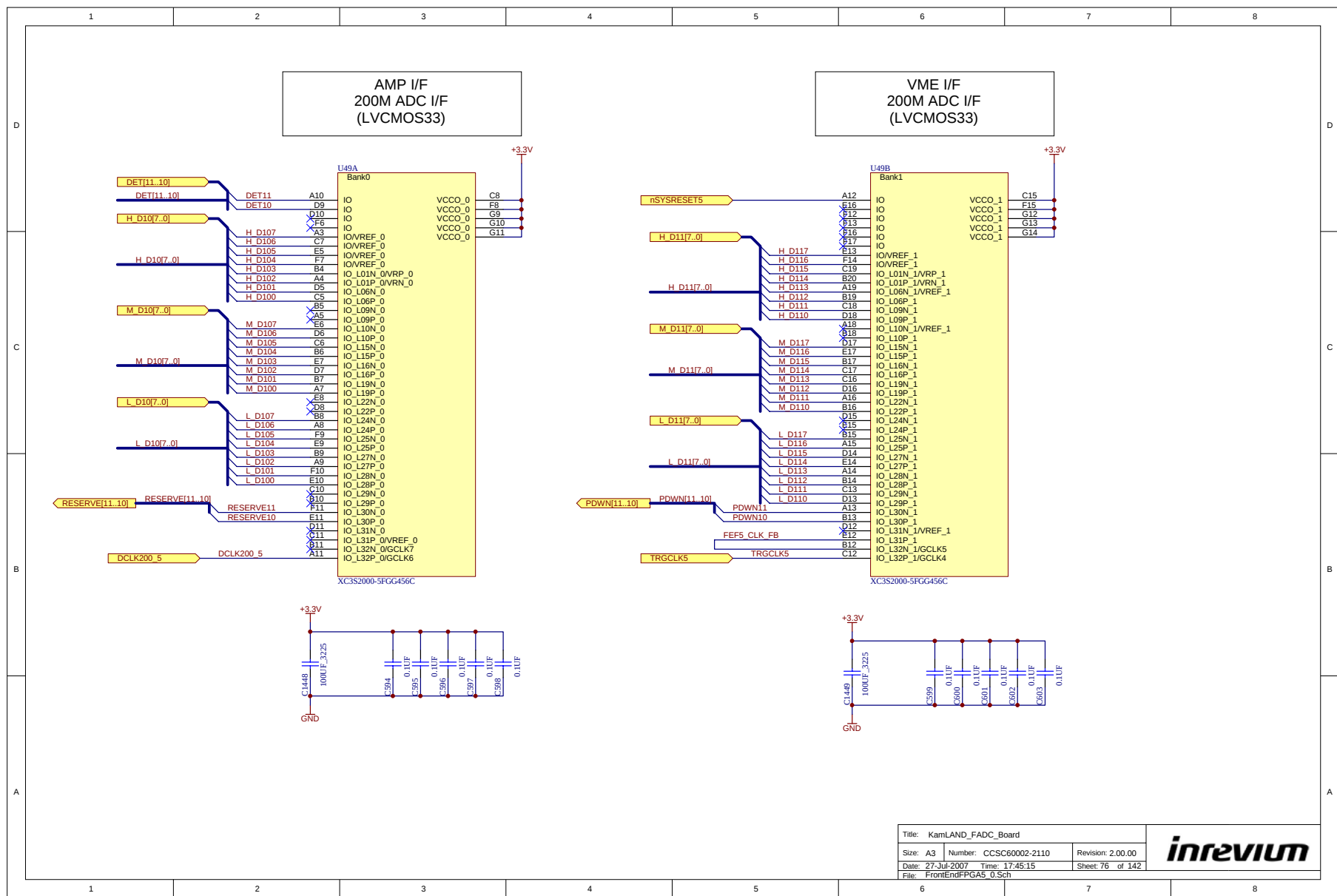


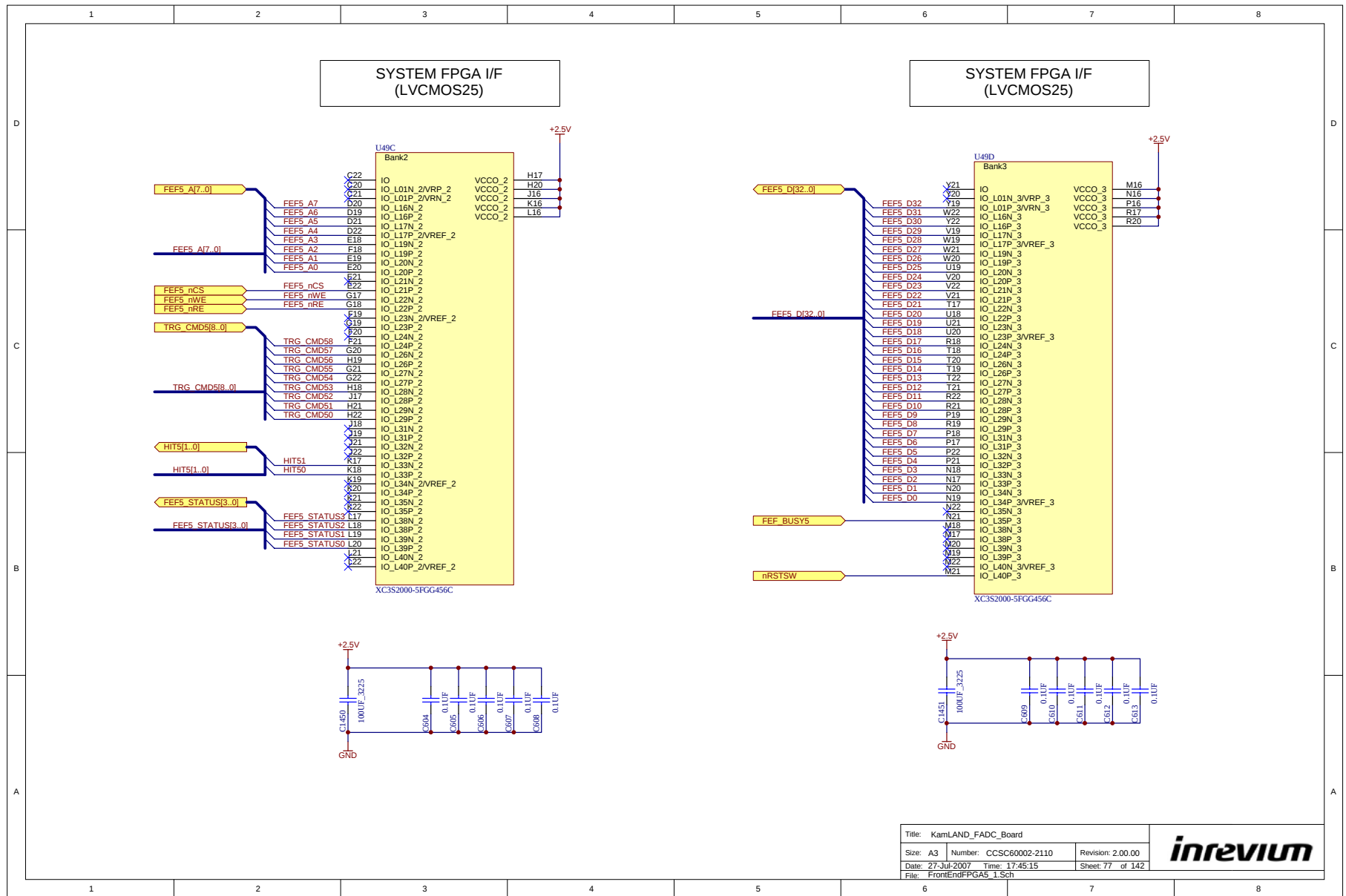


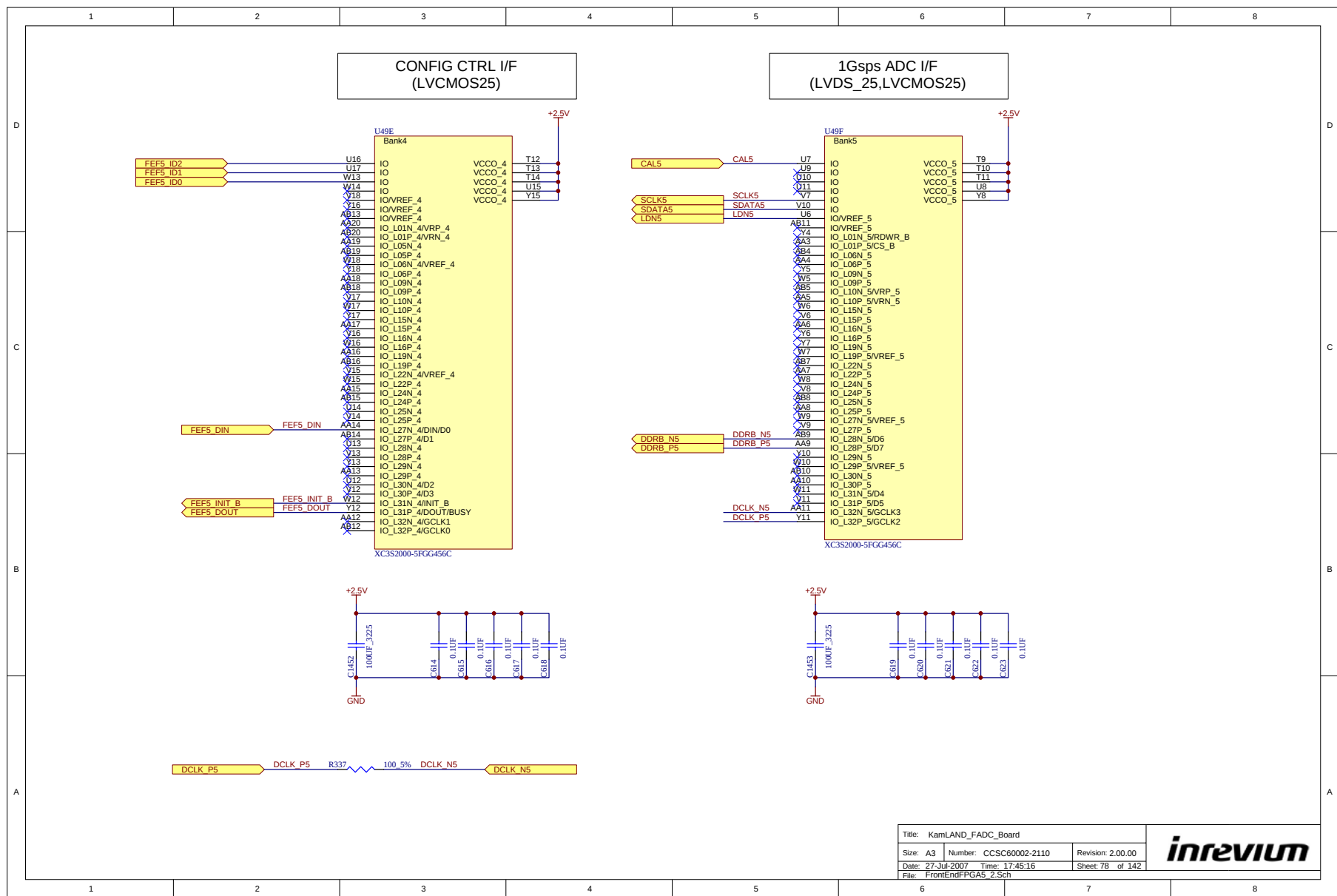


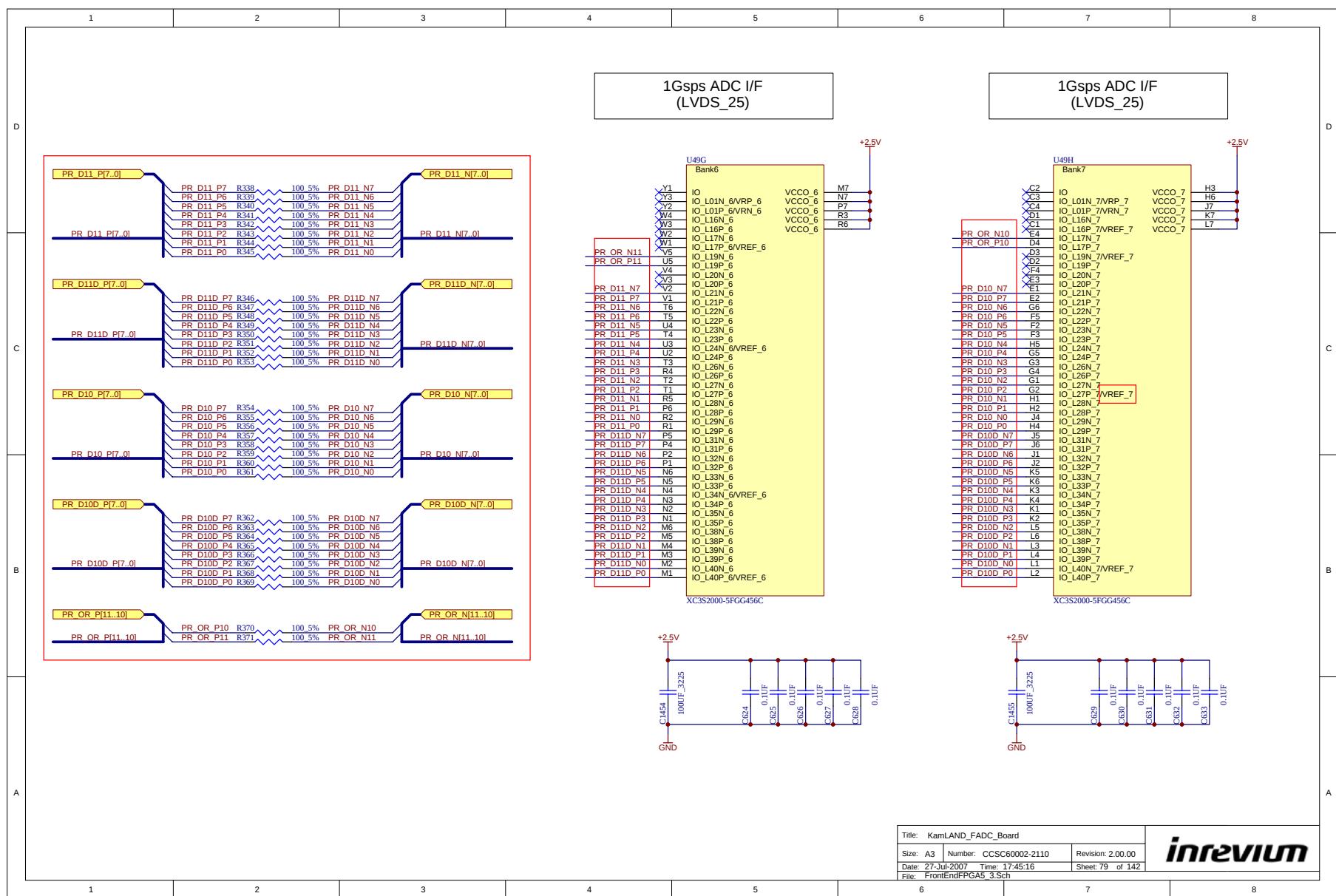
FrontEnd FPGA 5
TOP

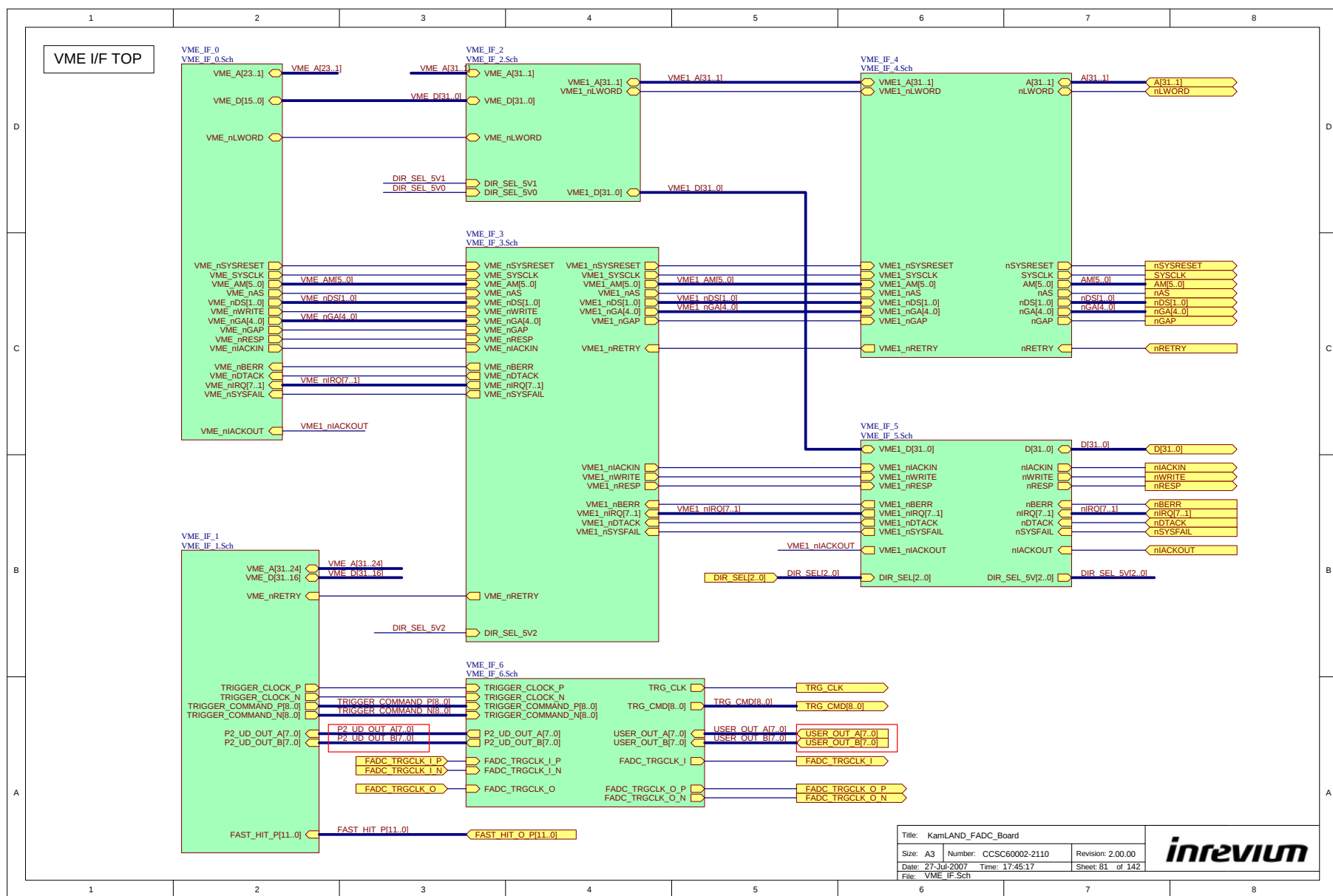


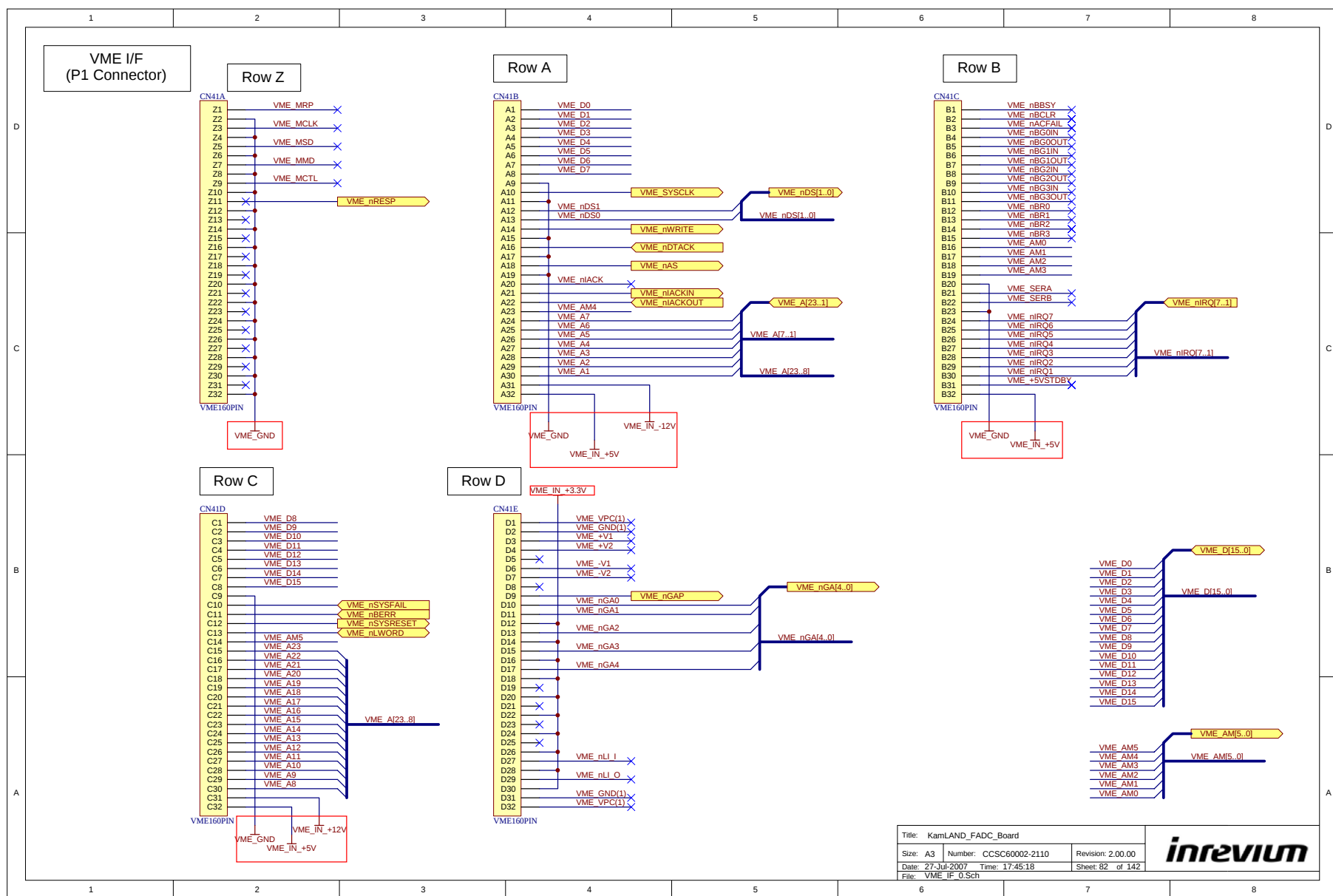


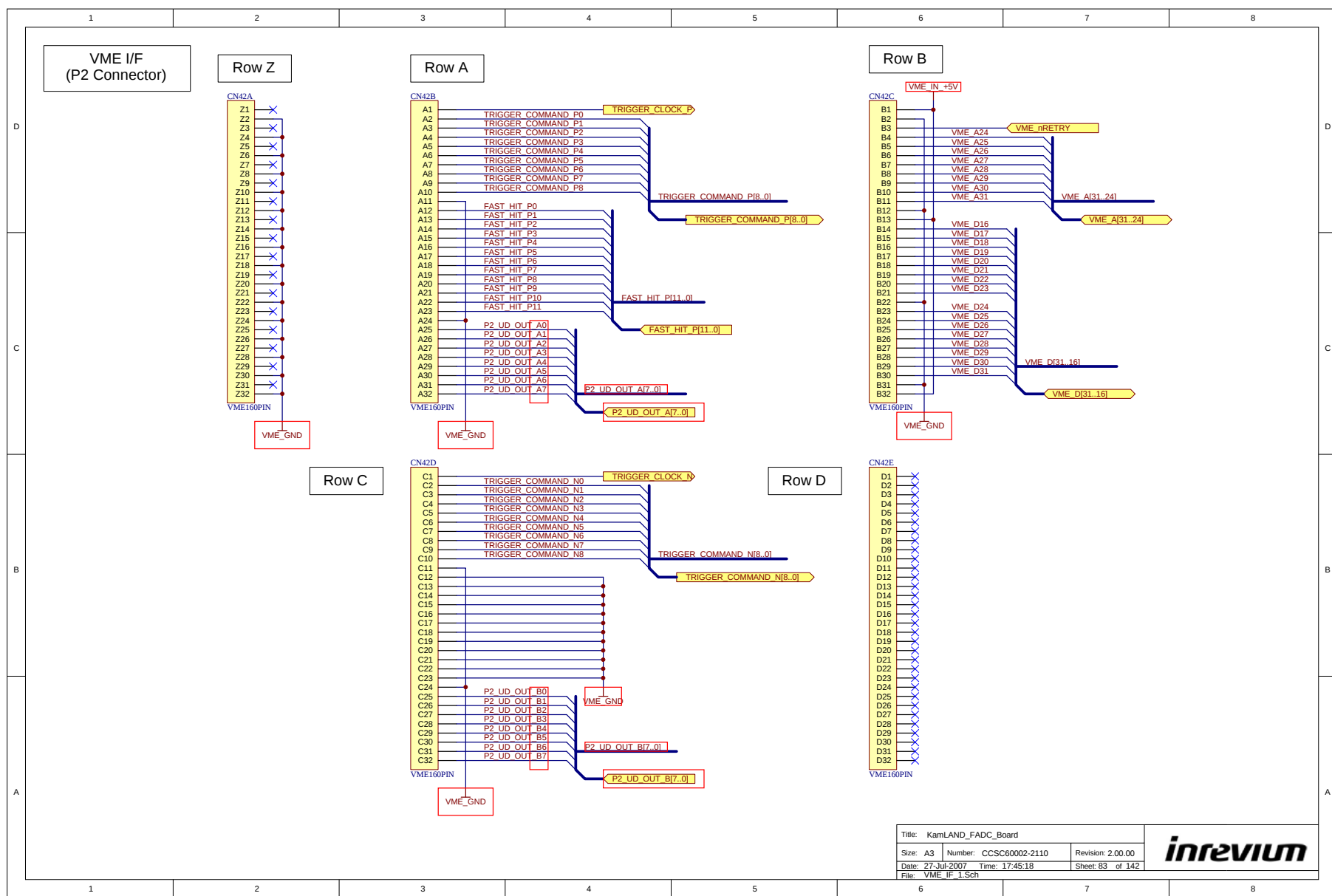


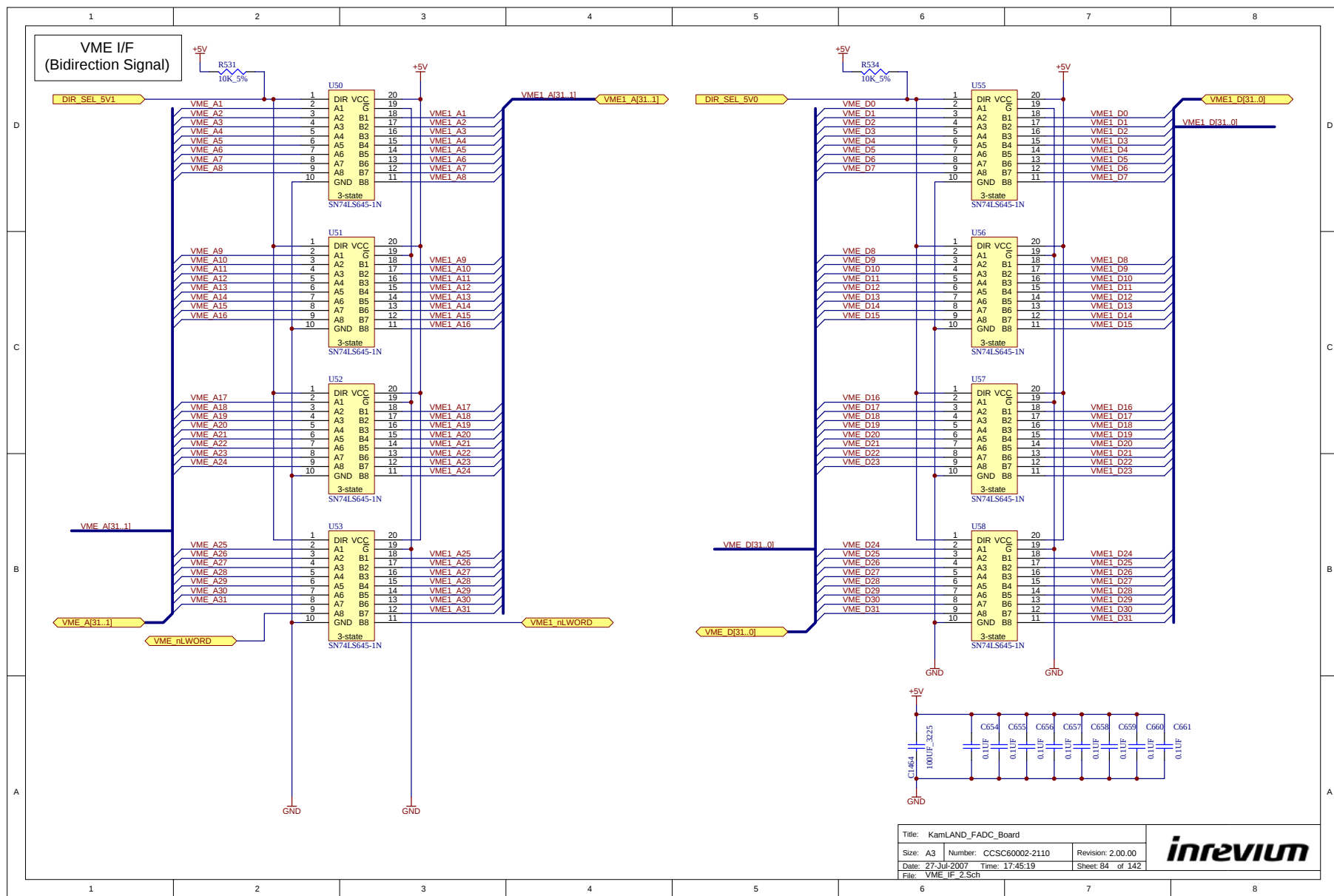


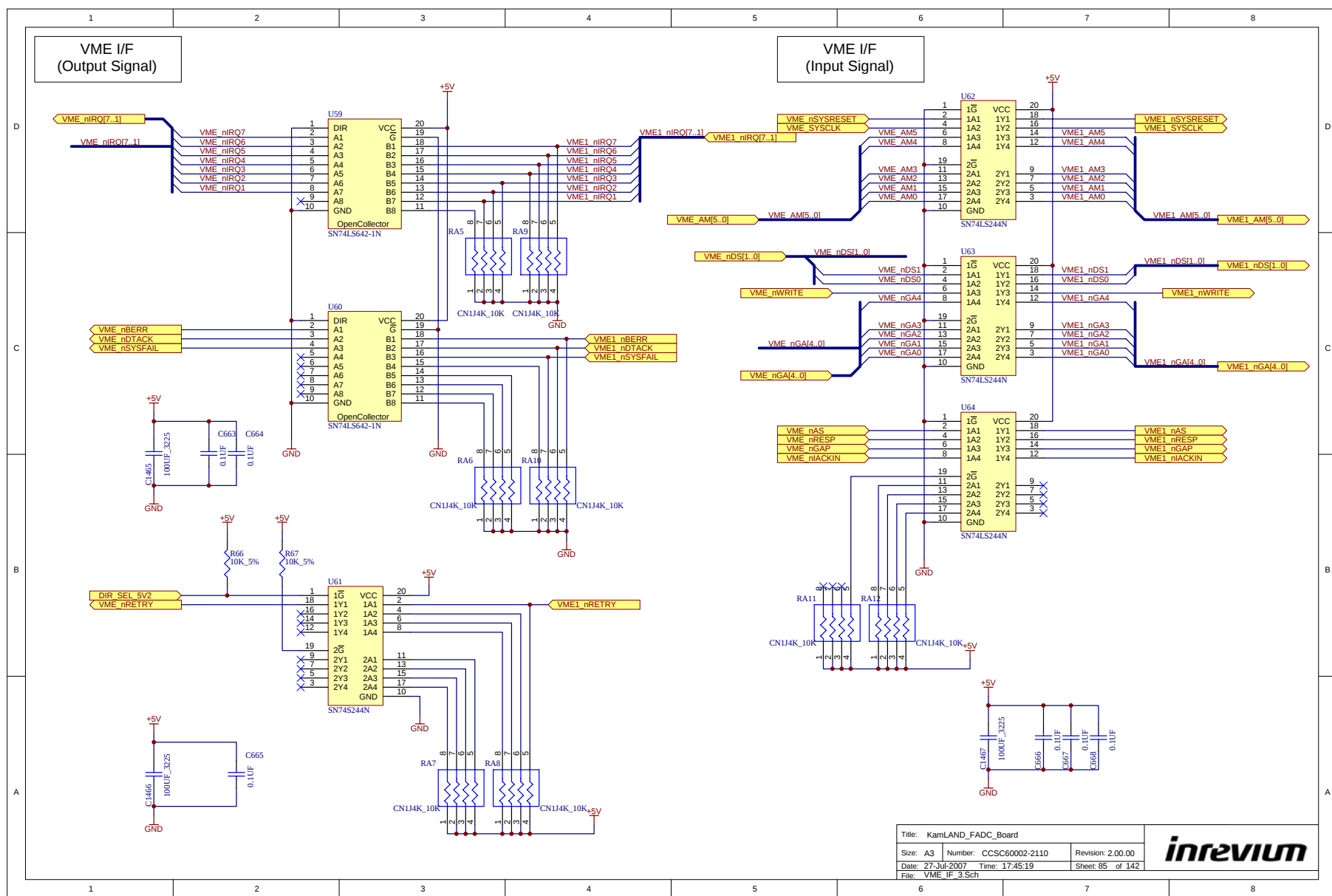




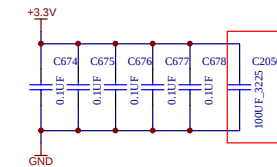
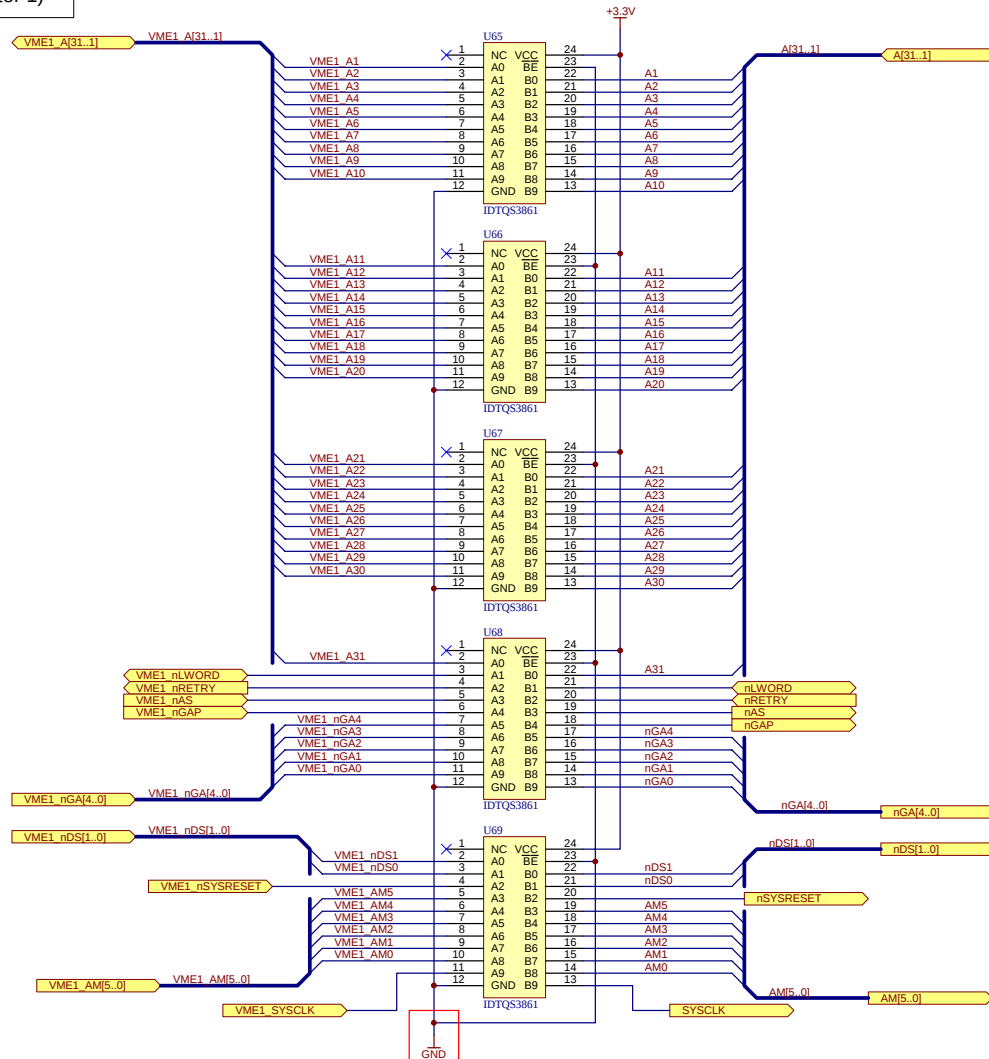




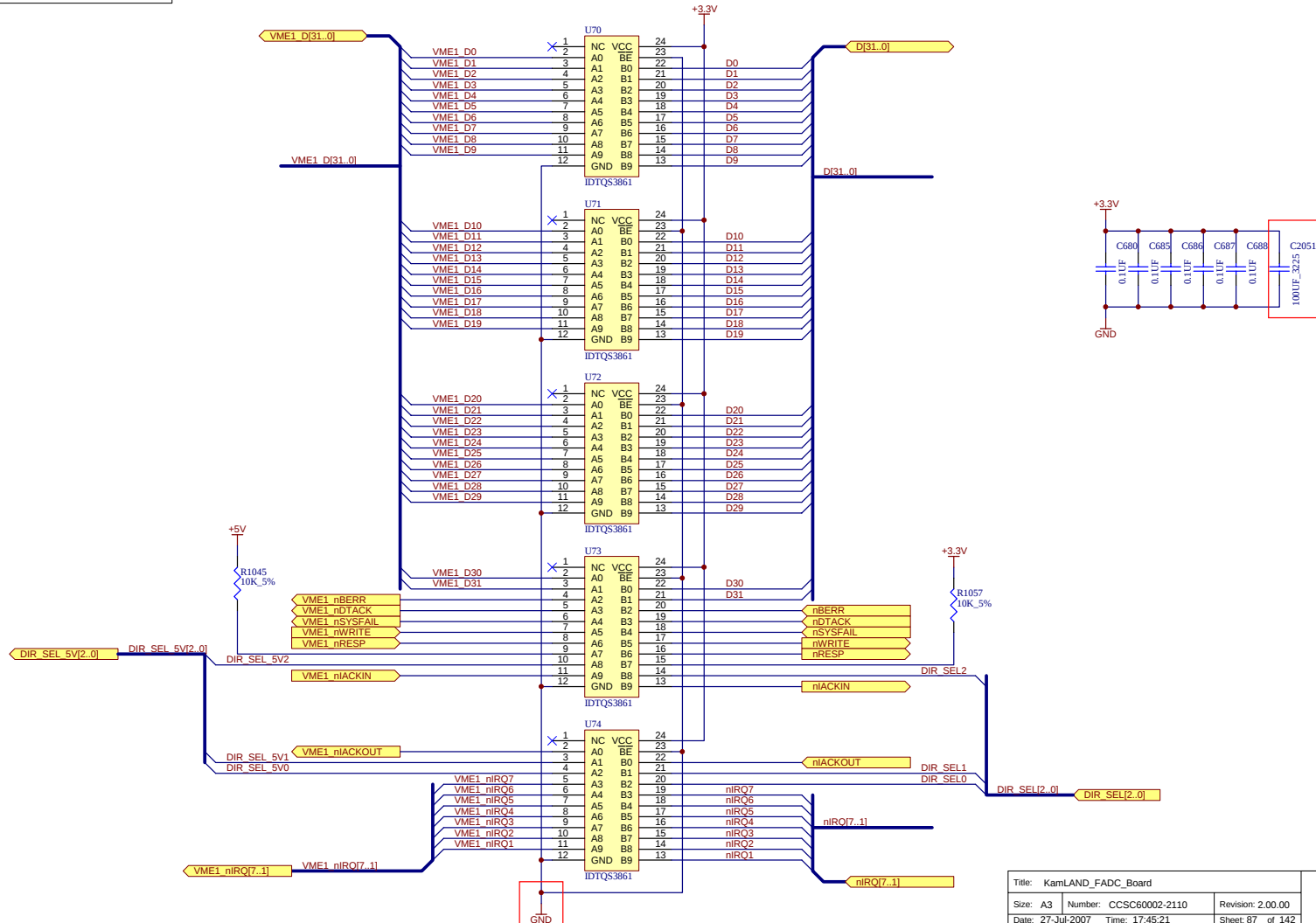




VME I/F
(Level Shifter 1)

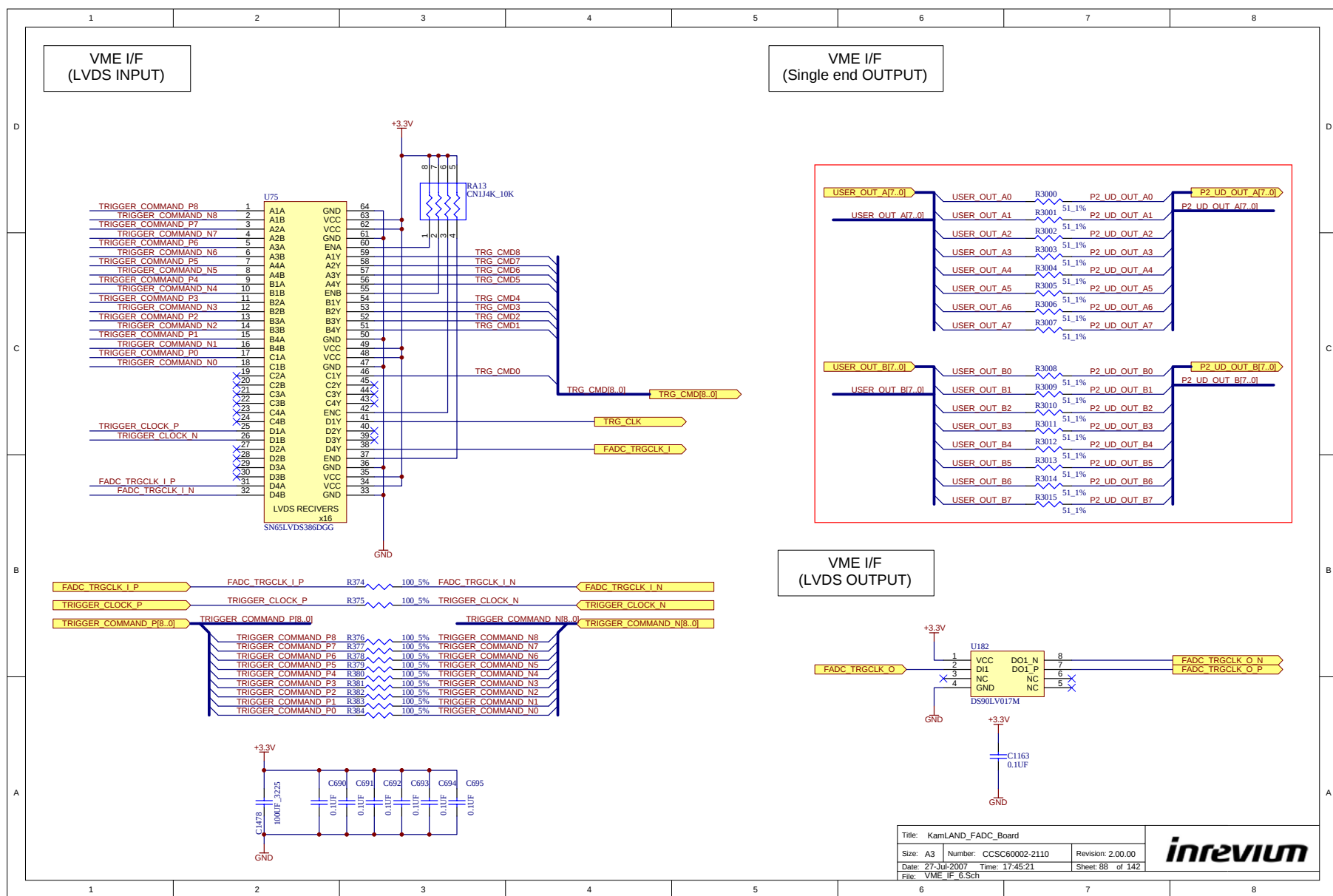


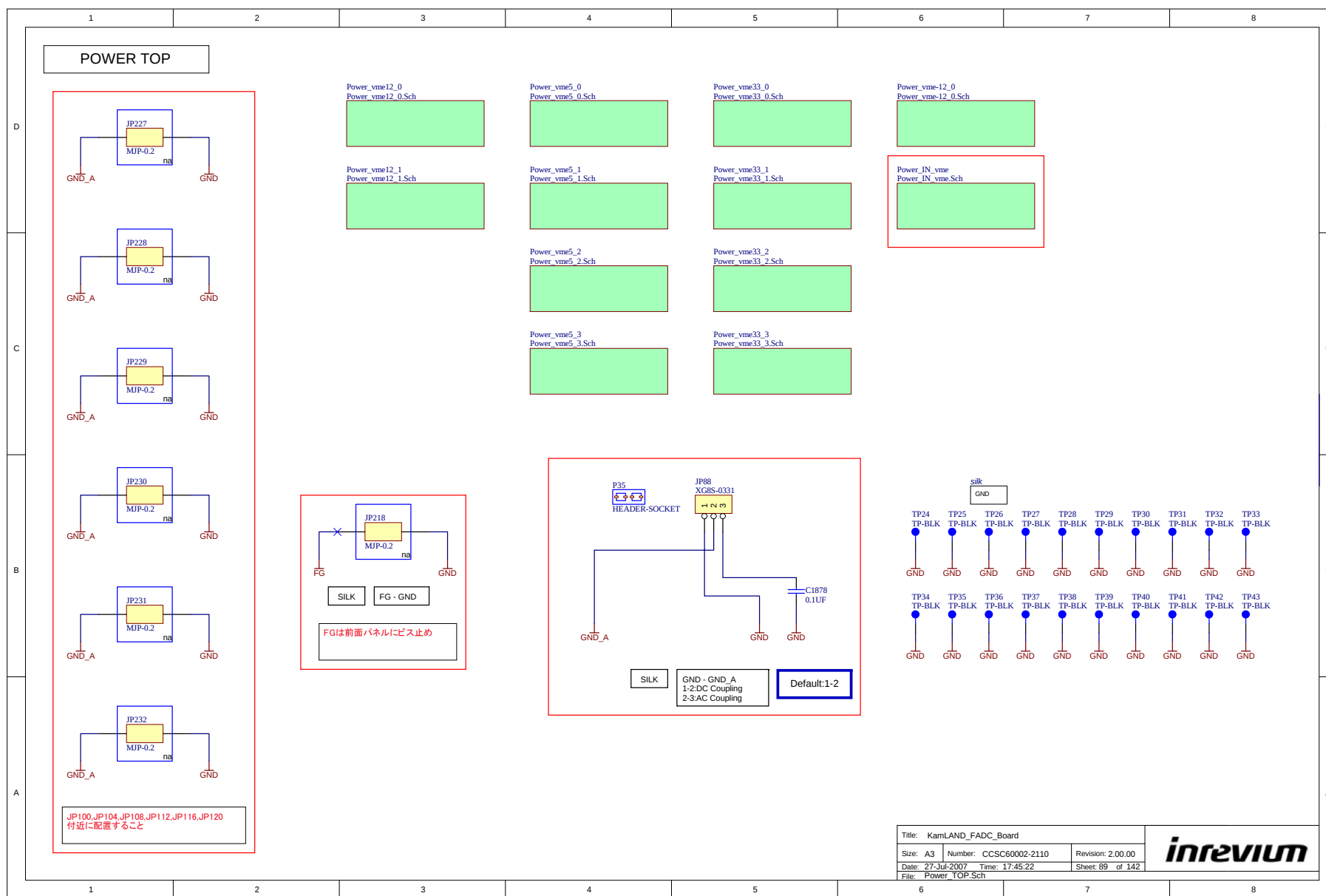
VME I/F
(Level Shifter 2)

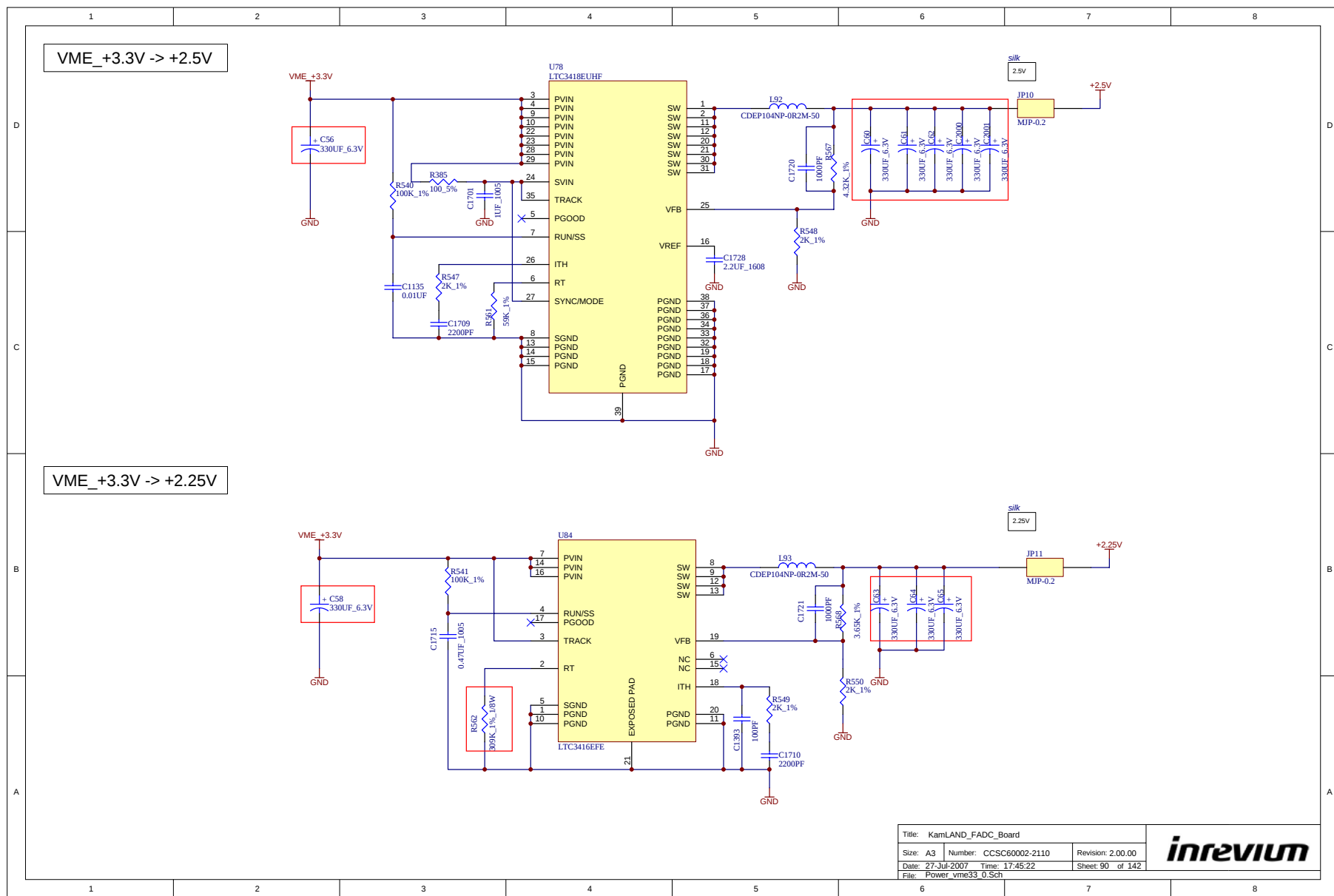


Title: KamLAND_FADC_Board	
Size: A3	Number: CCSC60002-2110
Date: 27-Jul-2007	Time: 17:45:21
File: VME_I/F_5.Sch	Sheet: 87 of 142

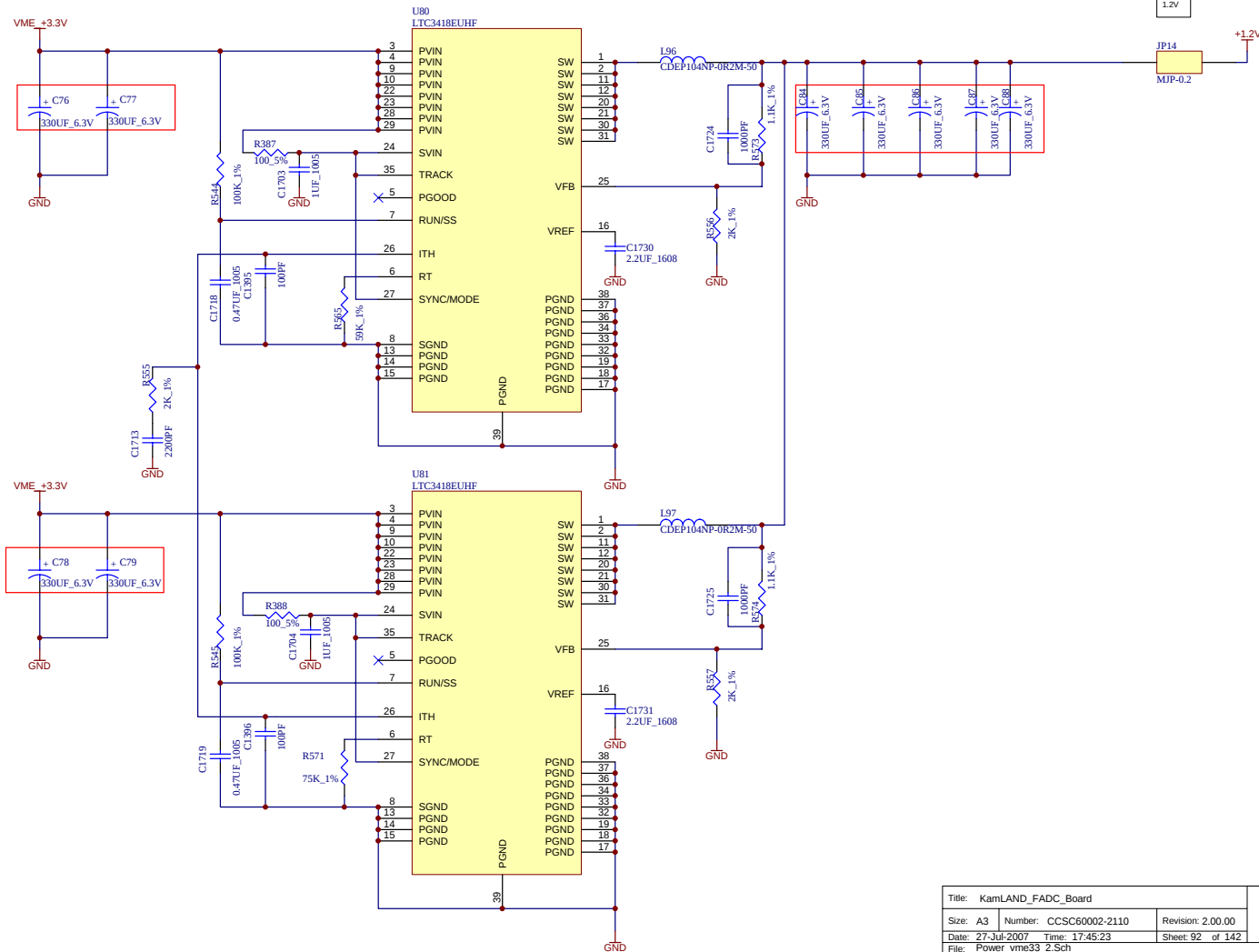
inrevium







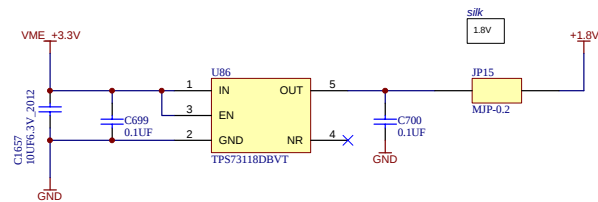
VME_+3.3V -> +1.2V



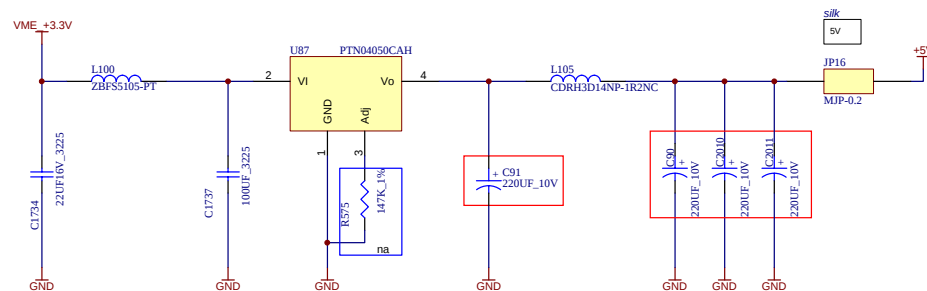
Title: KamLAND_FADC_Board	
Size: A3	Number: CCSC60002-2110
Date: 27-Jul-2007	Time: 17:45:23
File: Power_vme33_2.Sch	Sheet: 92 of 142

inrevium

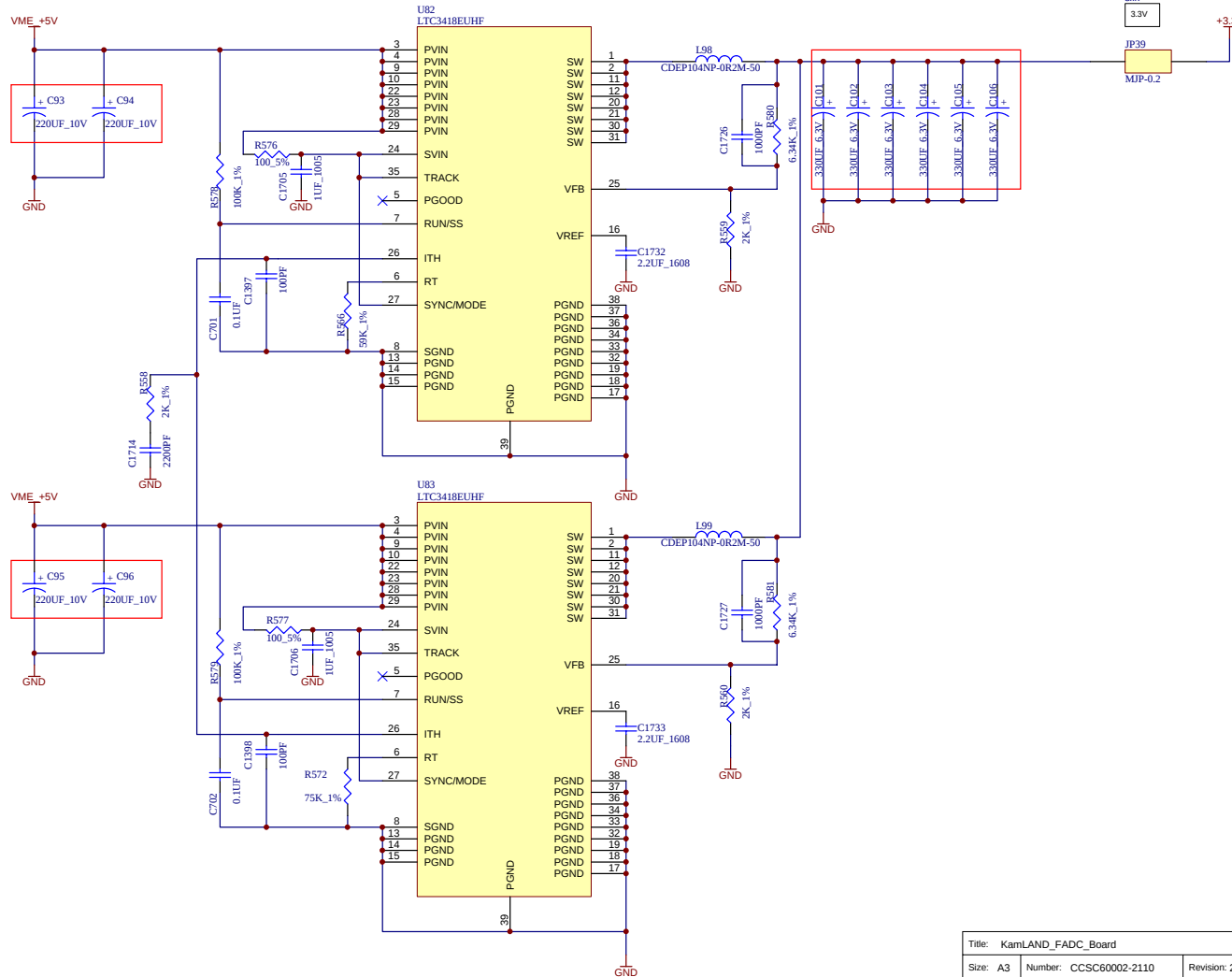
VME_+3.3V -> +1.8V



VME_+3.3V -> +5V



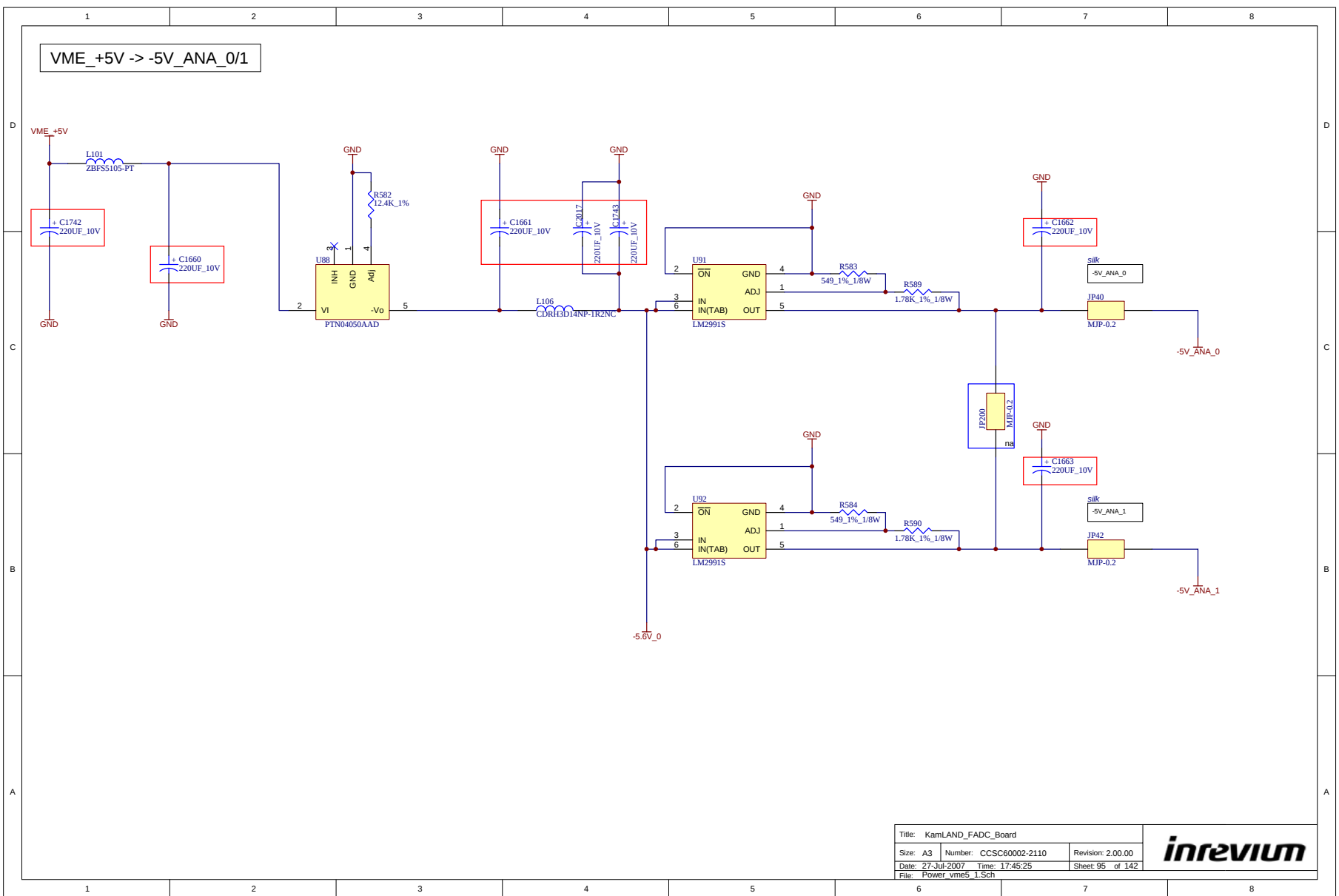
VME_+5V -> +3.3V



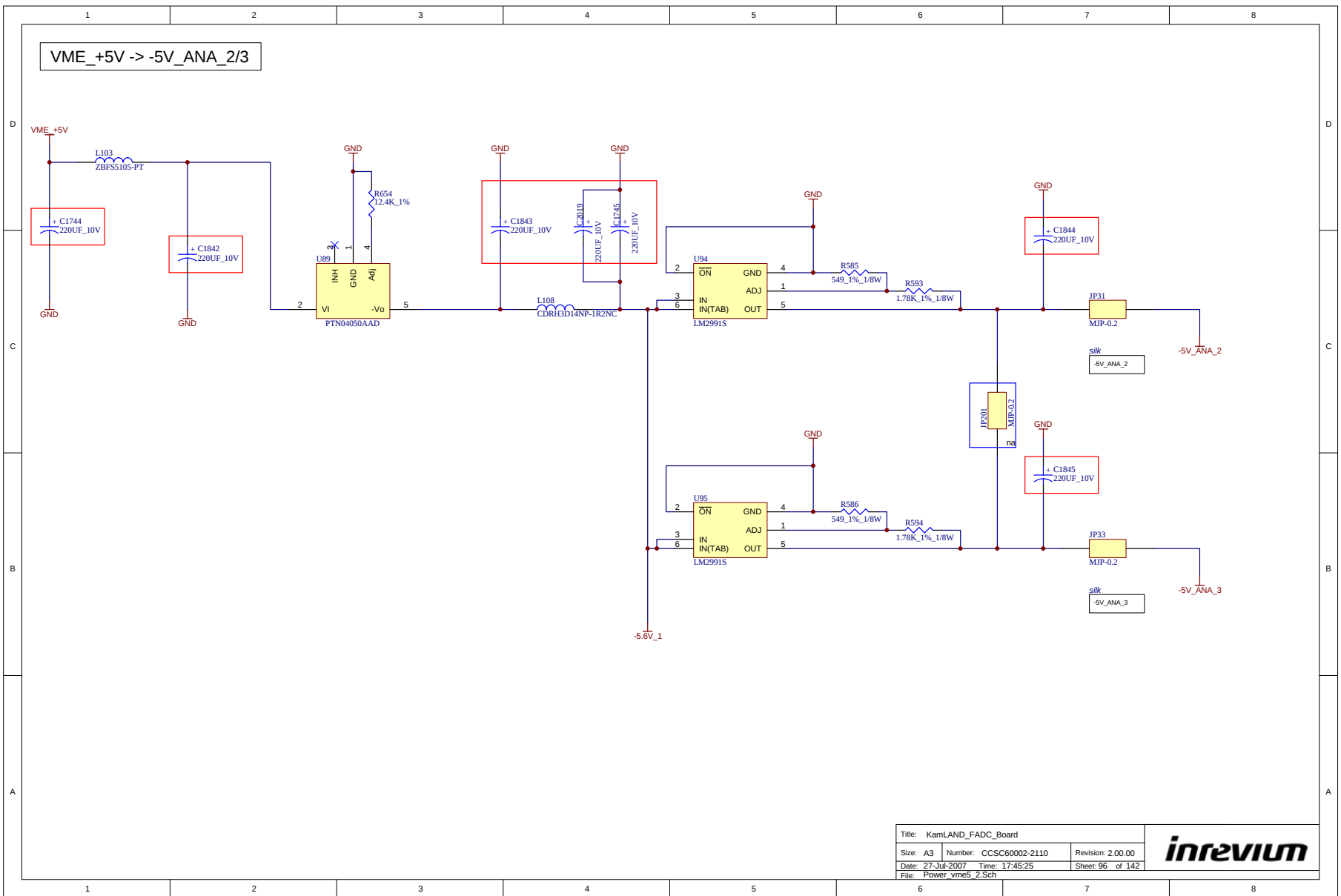
Title: KamLAND_FADC_Board		
Size: A3	Number: CCSC60002-2110	Revision: 2.00.00
Date: 27-Jul-2007	Time: 17:45:24	Sheet: 94 of 142
File: Power_vmes_0.Sch		

inrevium

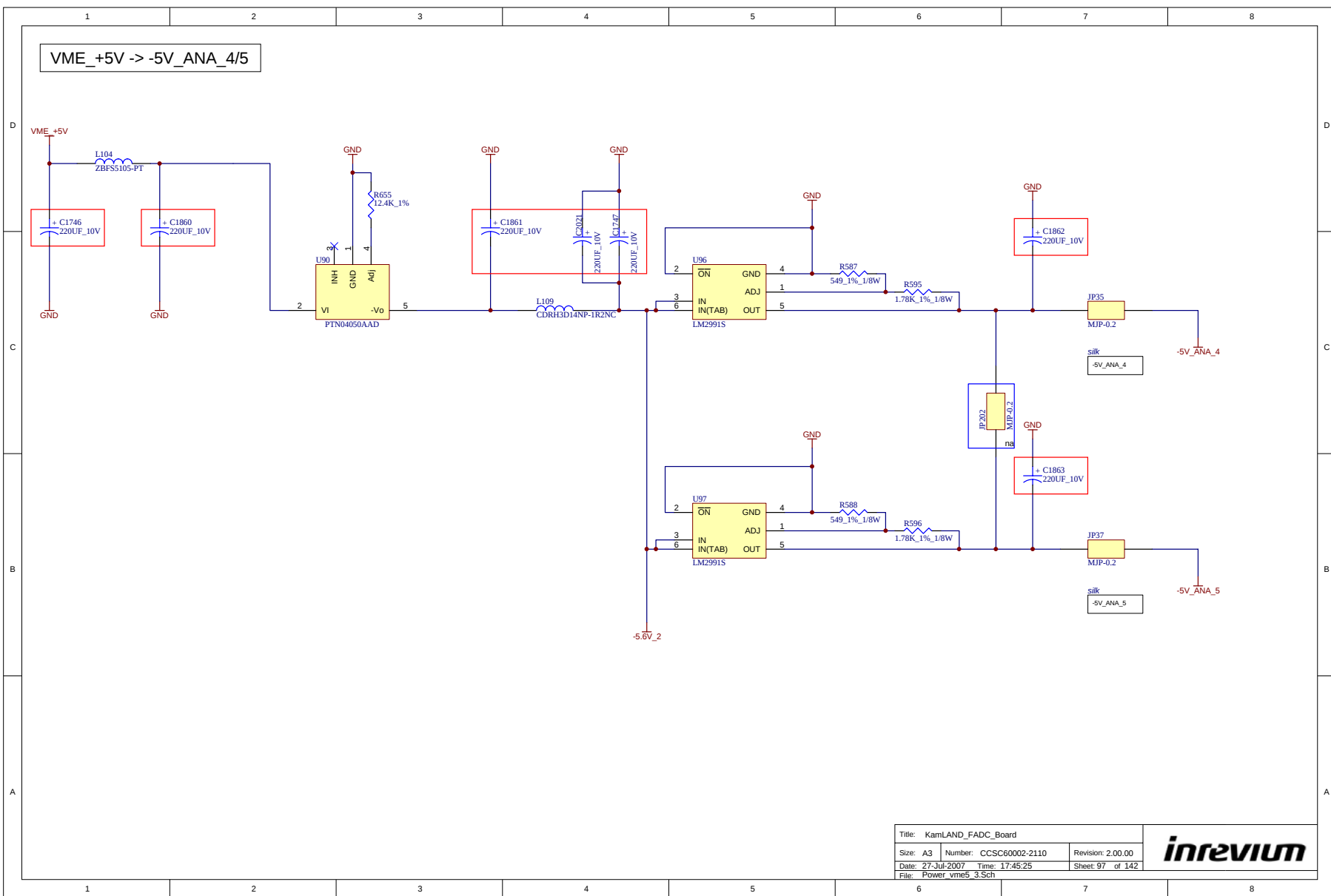
VME_+5V -> -5V_ANA_0/1



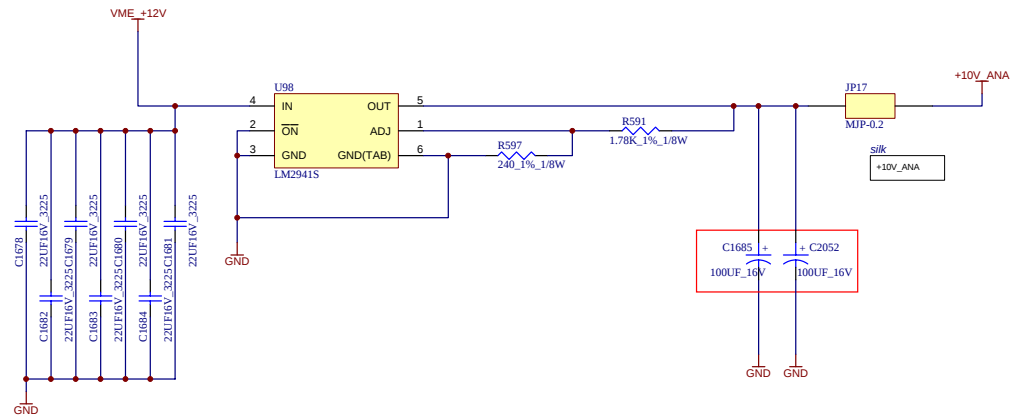
VME_+5V -> -5V_ANA_2/3



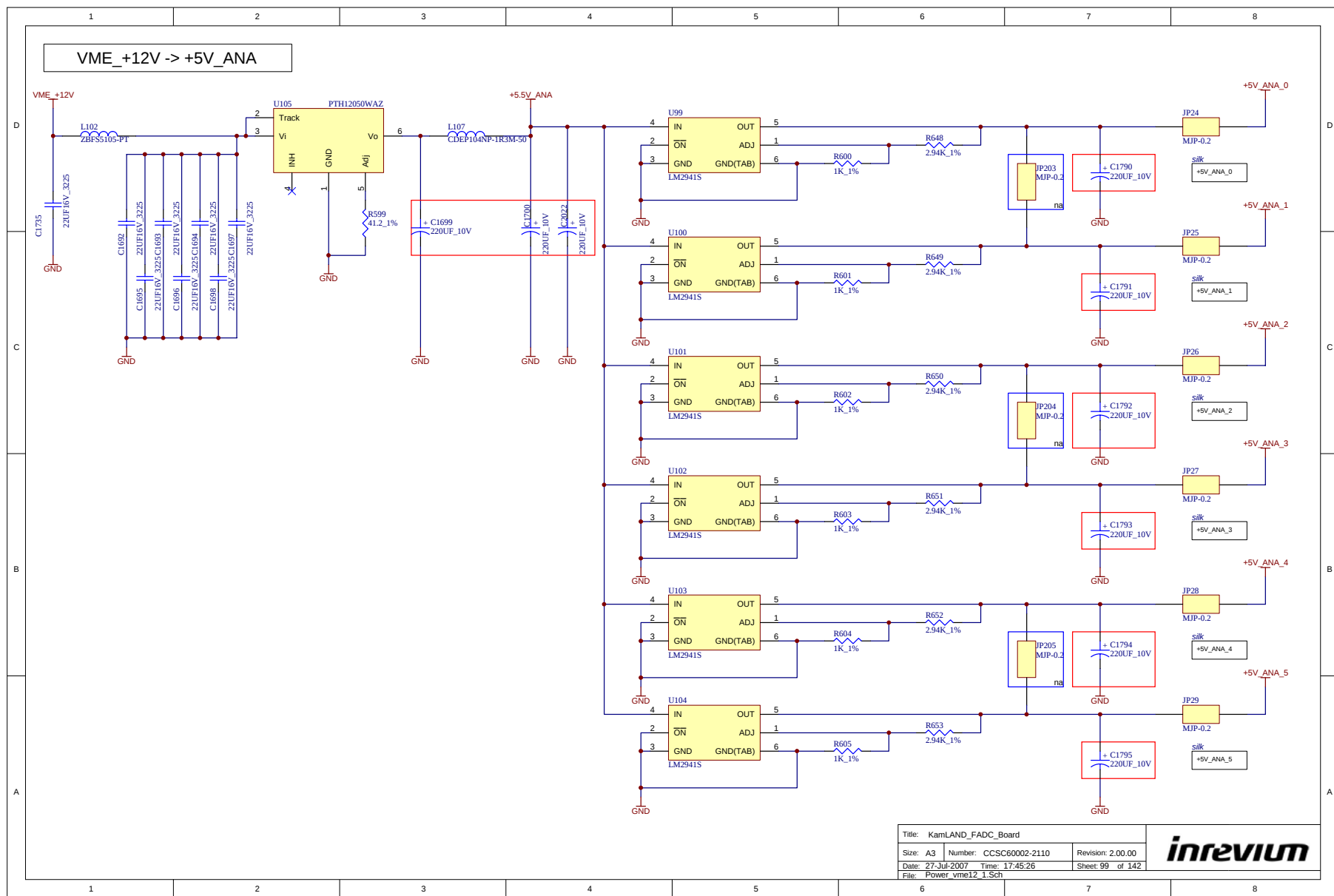
VME_+5V -> -5V_ANA_4/5



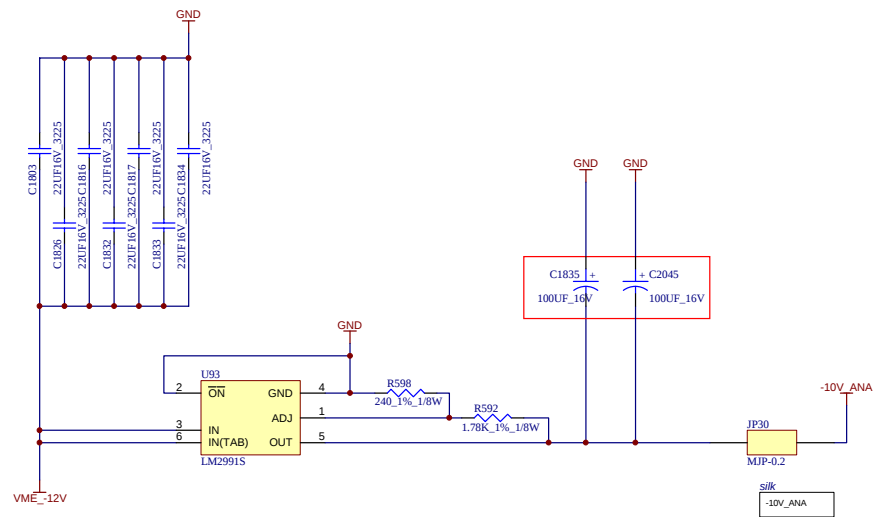
VME_+12V -> +10V_ANA



Title: KamLAND_FADC_Board			inrevium
Size: A3	Number: CCSC60002-2110	Revision: 2.00.00	
Date: 27-Jul-2007	Time: 17:45:26	Sheet: 98 of 142	
File: Power_vme12_0.Sch			



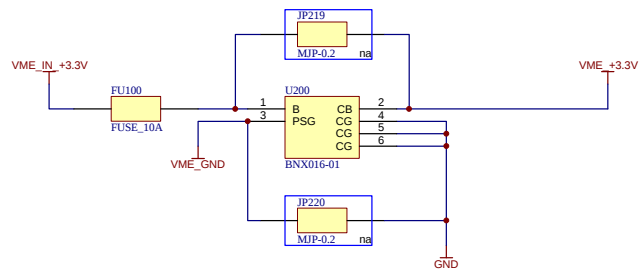
VME_-12V -> -10V_ANA



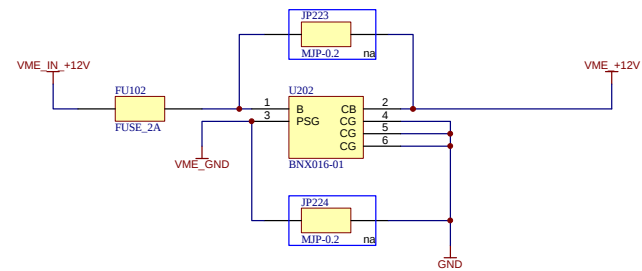
Title: KamLAND_FADC_Board		
Size: A3	Number: CCSC60002-2110	Revision: 2.00.00
Date: 27-Jul-2007	Time: 17:45:27	Sheet: 100 of 142
File: Power_vme-12_0.Sch		

inrevium

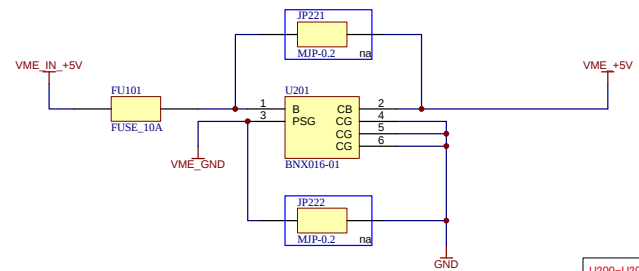
VME_IN_+3.3V -> VME_+3.3V



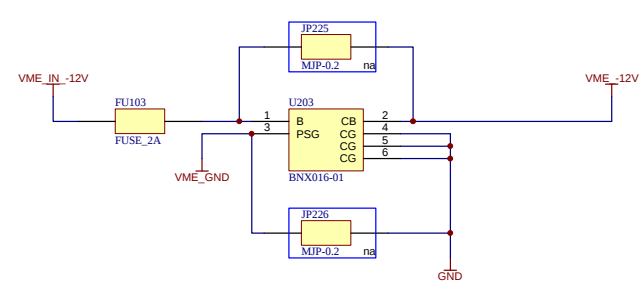
VME_IN_+12V -> VME_+12V



VME_IN_+5V -> VME_+5V

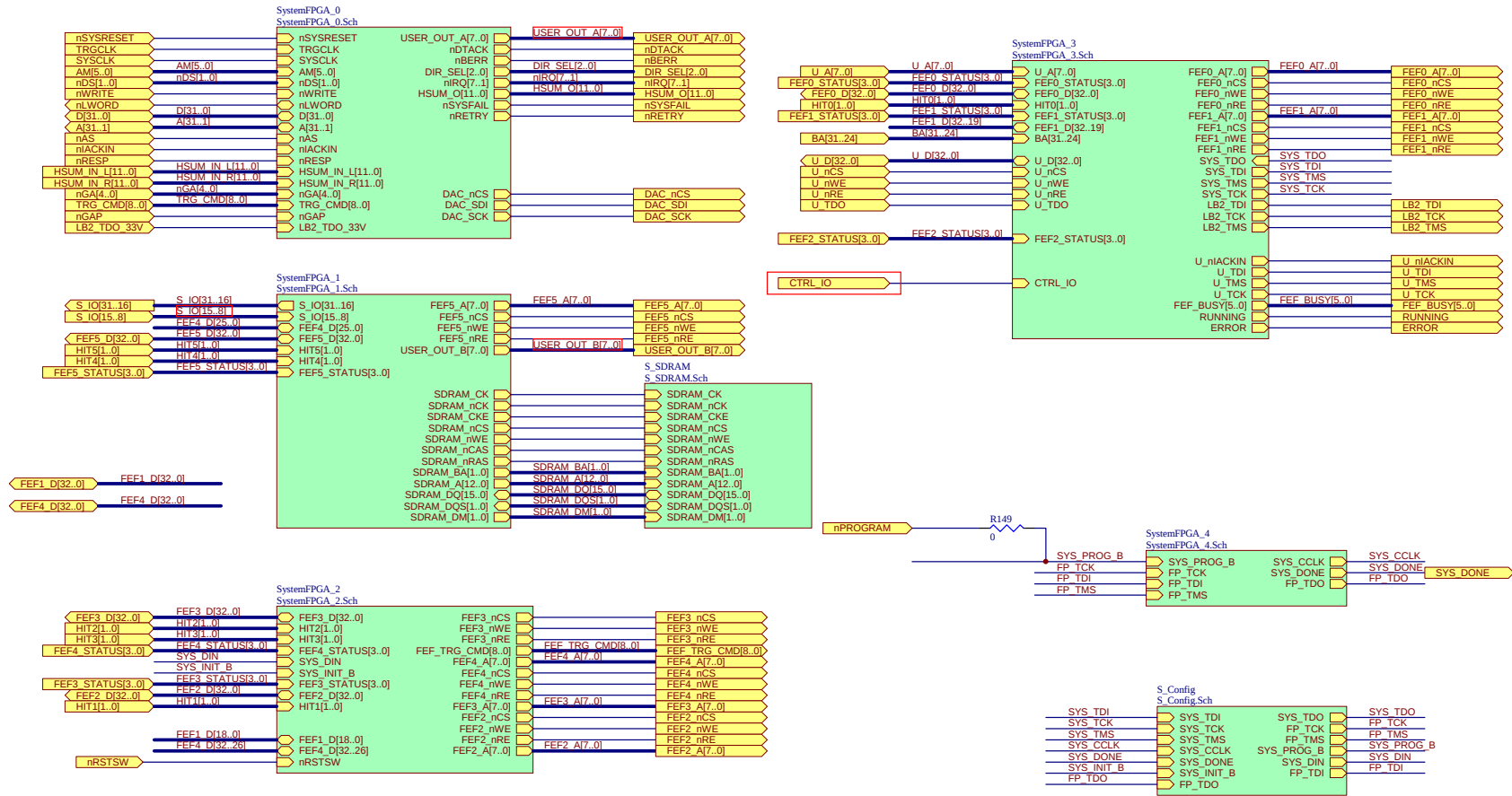


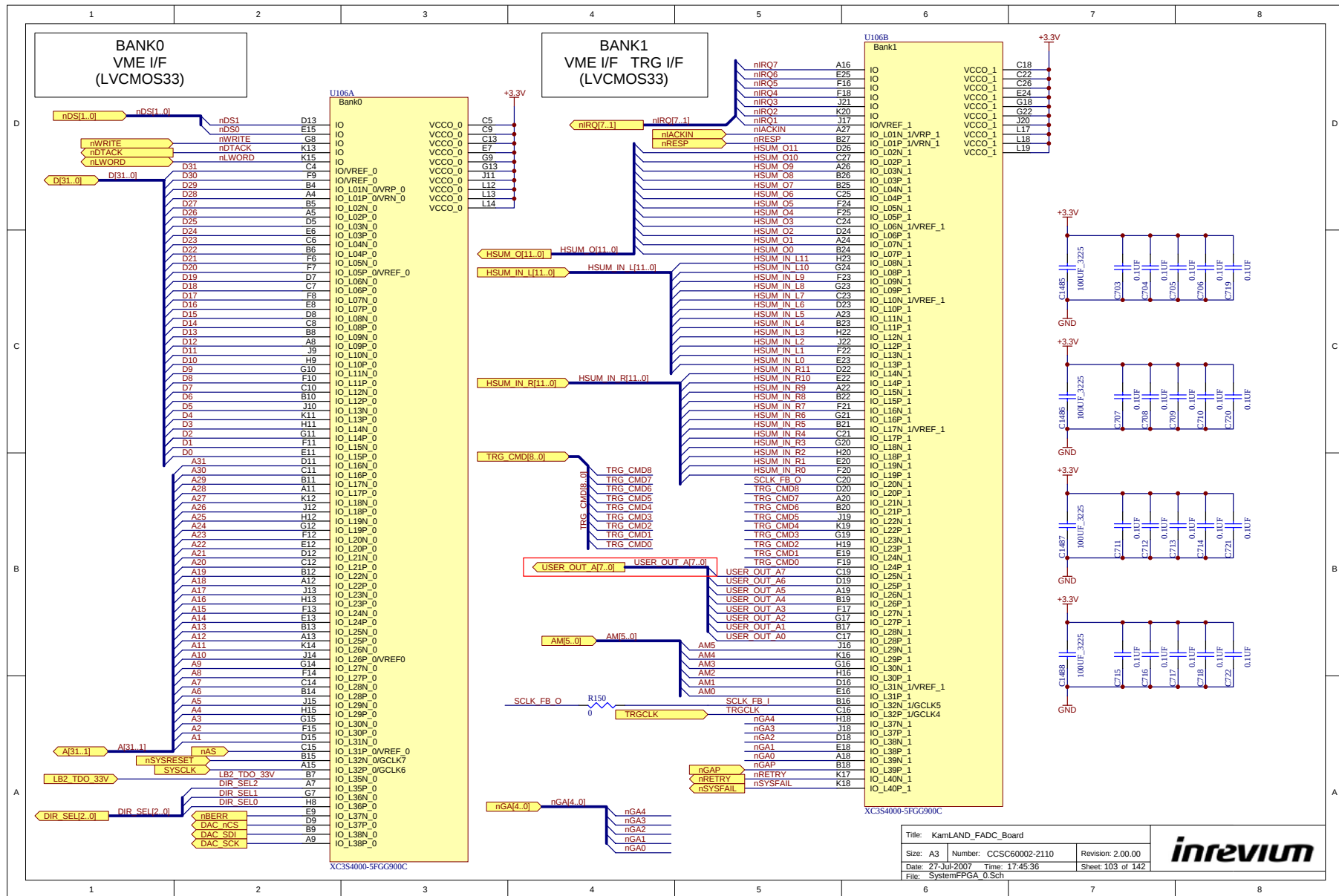
VME_IN_-12V -> VME_-12V

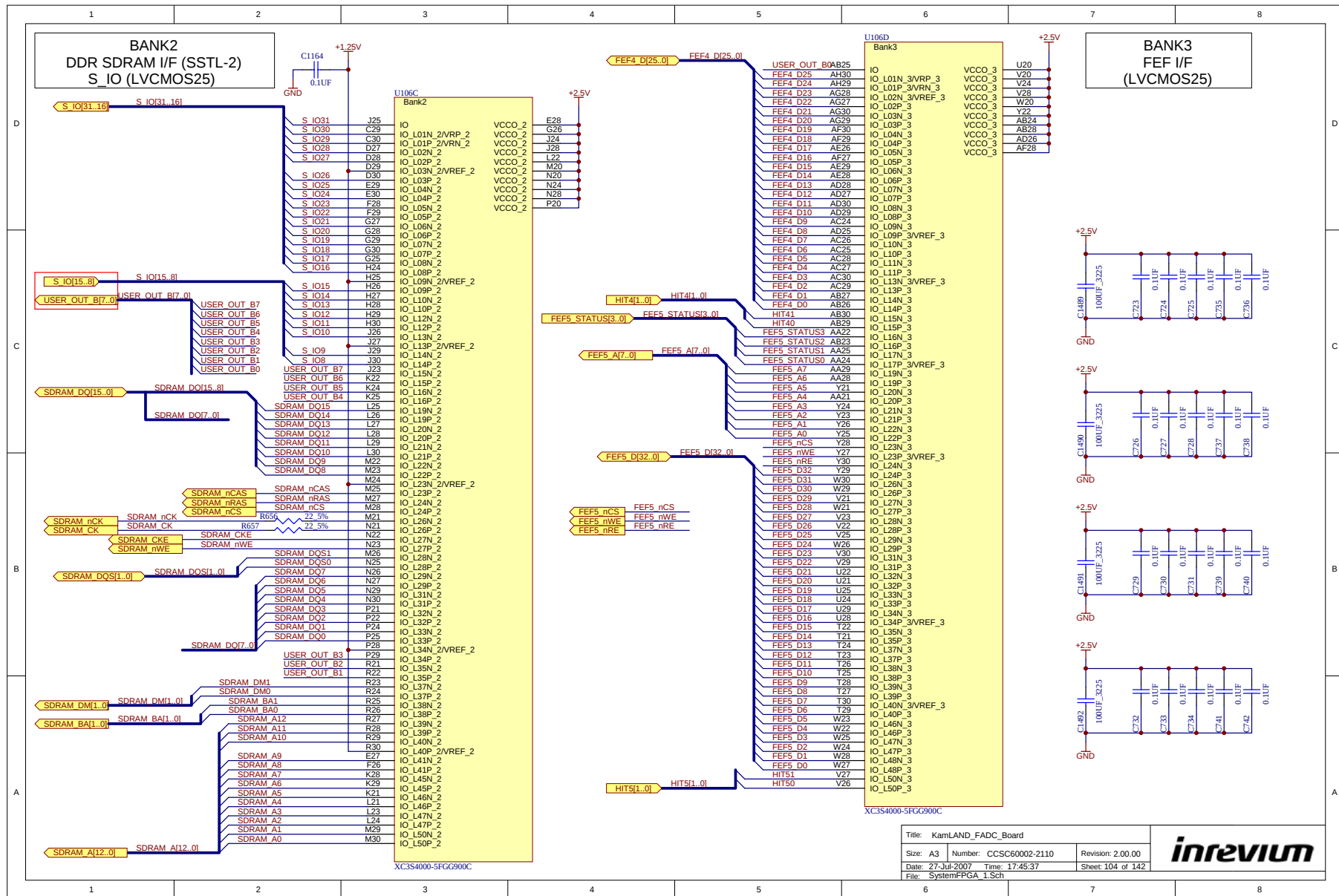


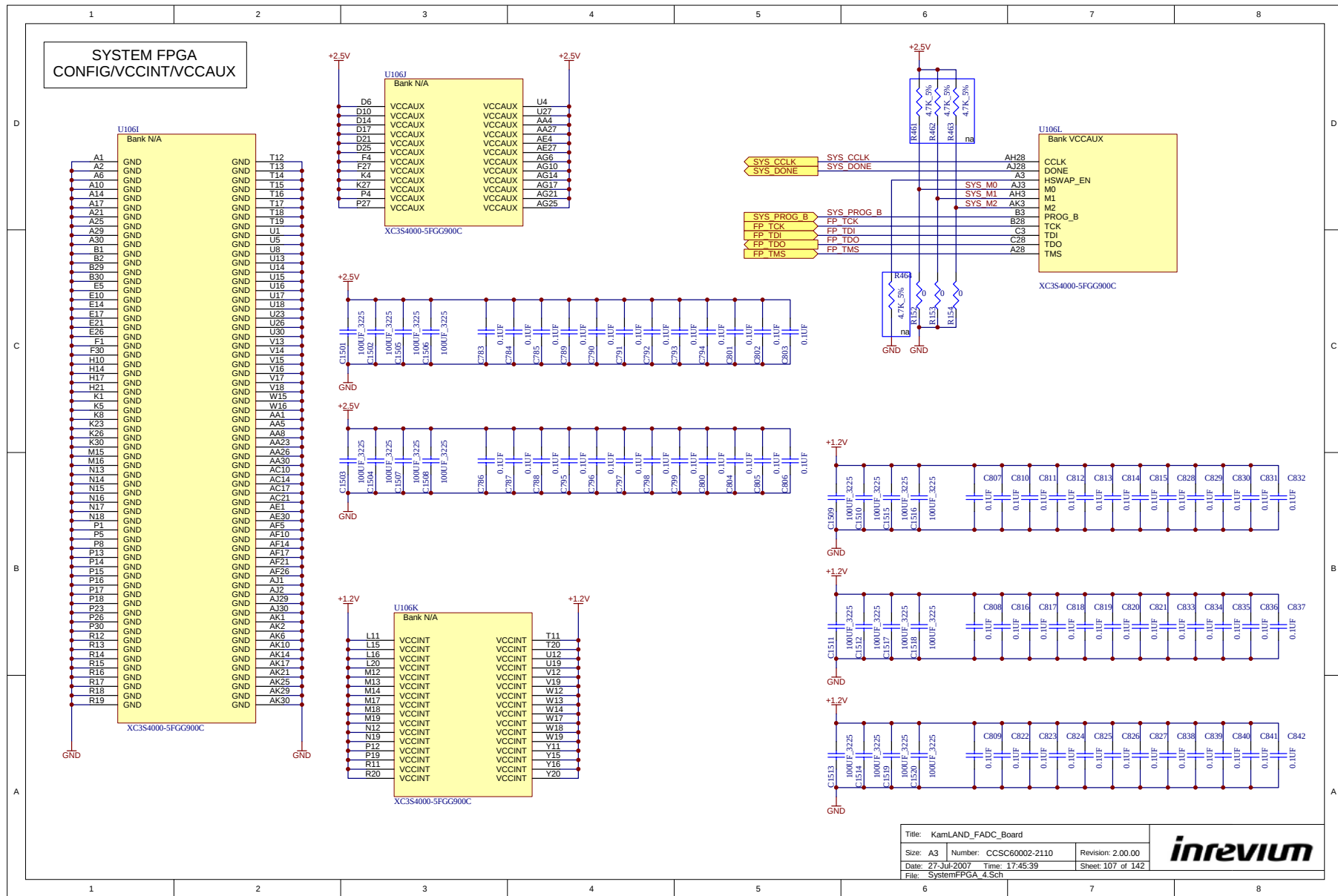
U200-U203の代わりに
MJP-02を実装できるようにしておく

SYSTEM FPGA TOP

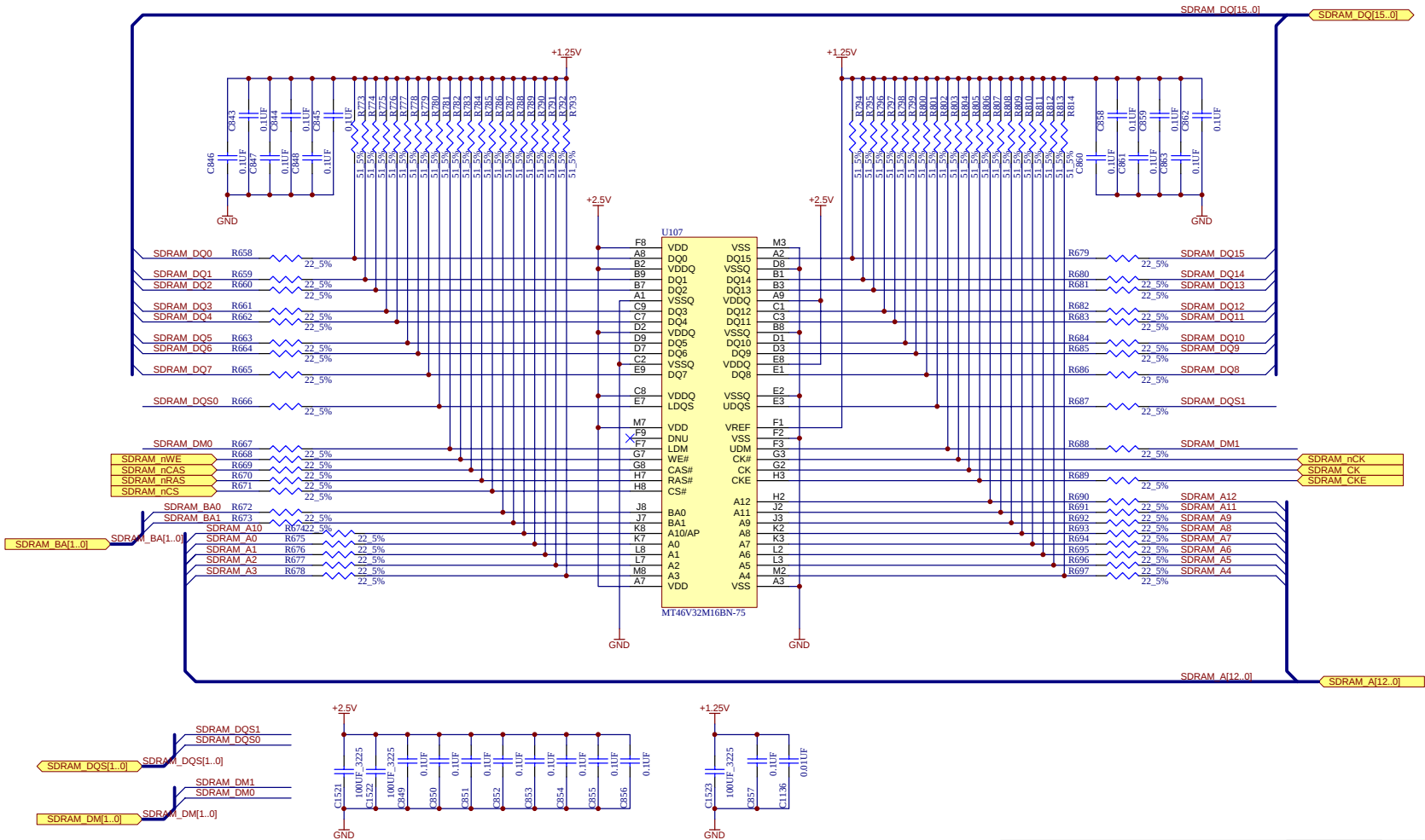








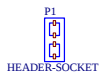
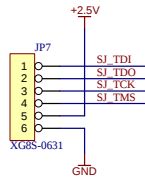
DDR SDRAM (SYSTEM FPGA)



SYSTEM FPGA PROM

SILK

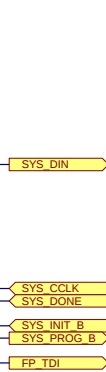
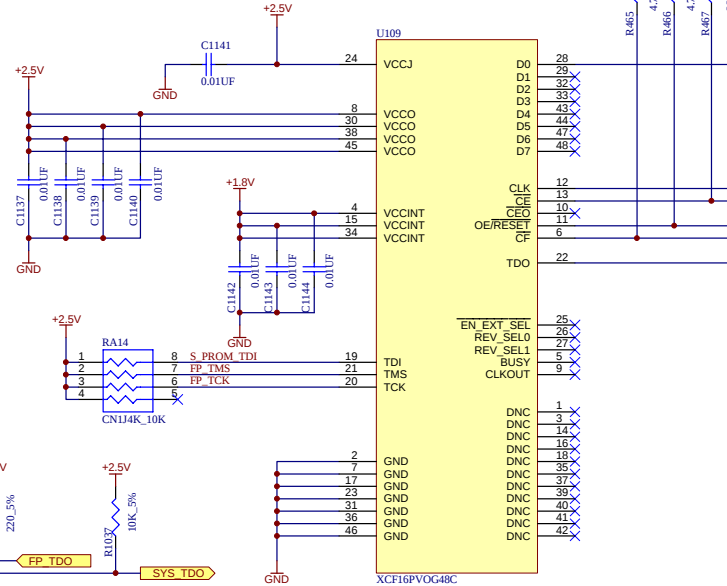
SFFPGA JTAG
1:T.DI
2:TDO
3:TCK
4:TMS
5:+2.5V
6:GND



SILK

1-2:S_JTAG
2-3:S_FPGA

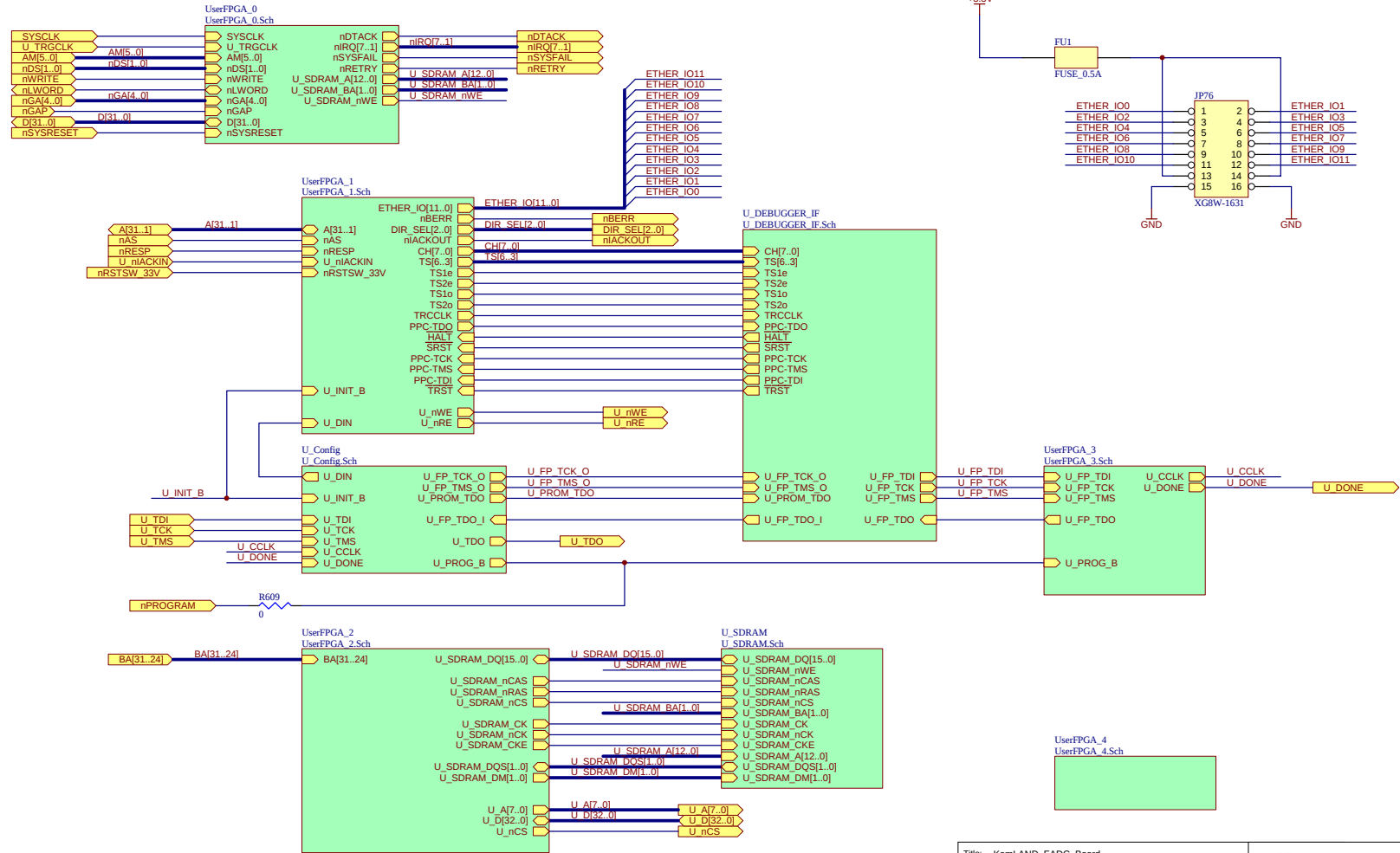
Default:1-2

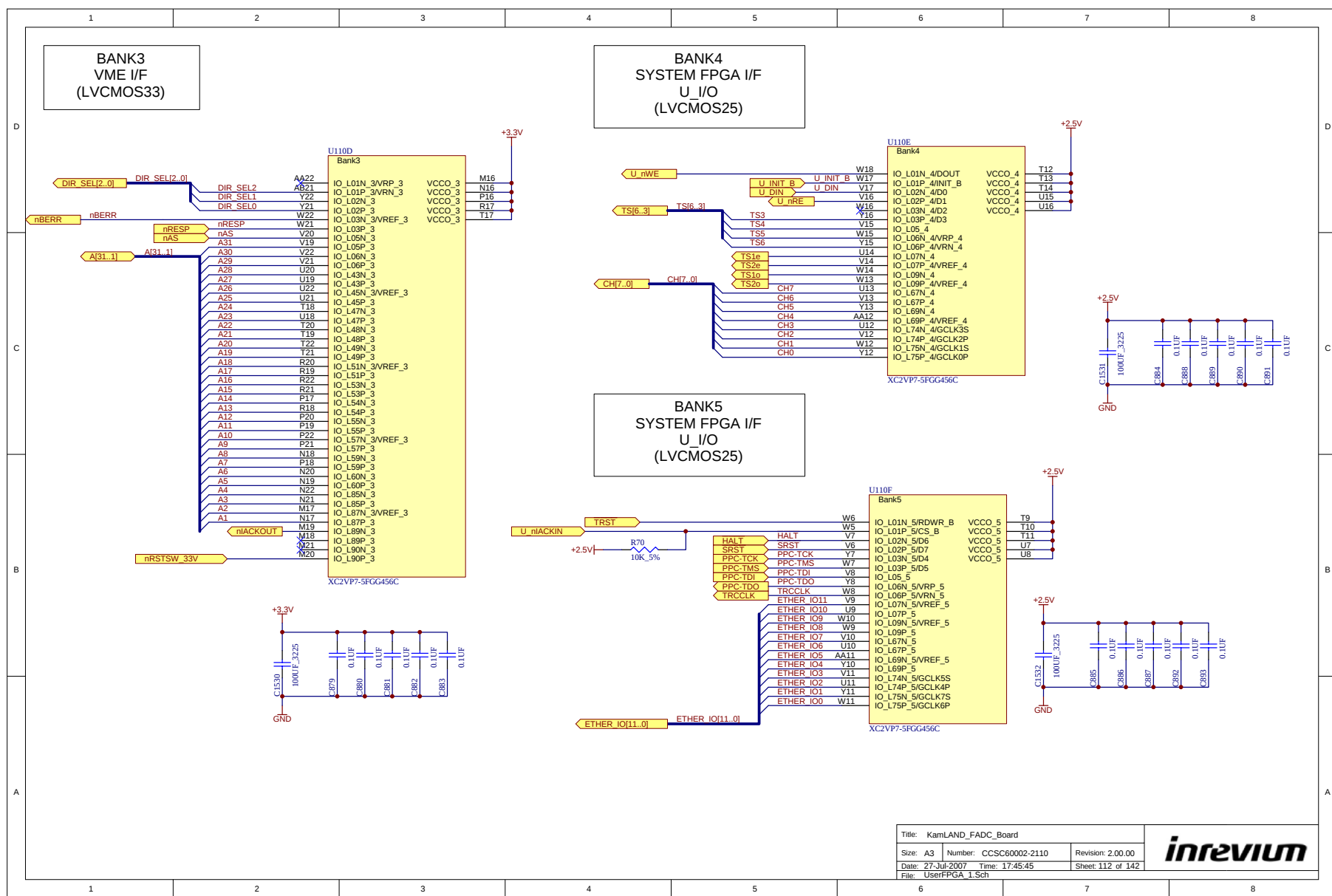


Title: KamLAND_FADC_Board		
Size: A3	Number: CCSC60002-2110	Revision: 2.00.00
Date: 27-Jul-2007	Time: 17:45:40	Sheet: 109 of 142
File: S_Config.Sch		

inrevium

USER FPGA TOP





Title: KamLAND_FADC_Board

Size: A3

Number: CCSC60002-2110

Revision: 2.00.00

Date: 27-Jul-2007

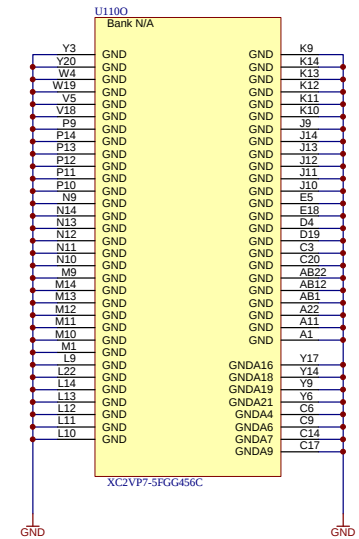
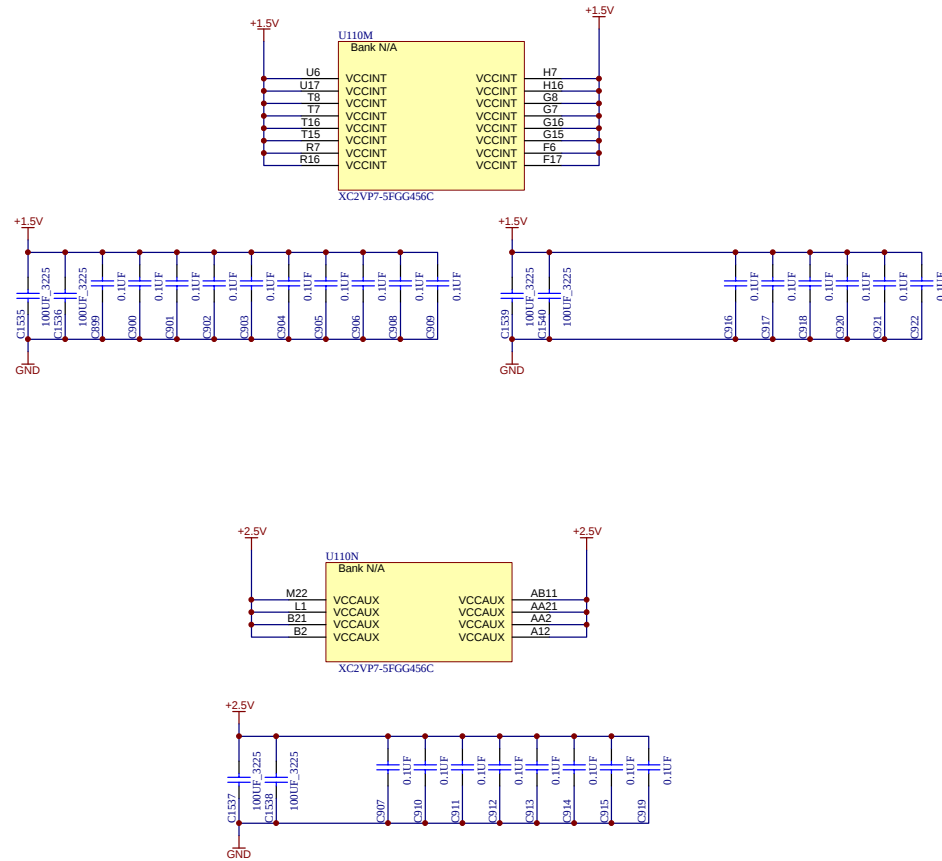
Time: 17:45:45

Sheet: 112 of 142

File: UserFPGA_1.Sch

inrevium

USER FPGA
VCCINT/VCCAUX



USER FPGA PROM

SILK

UFGPA JTAG

1:T.DI
2:TDO
3:TCK
4:TMS
5:+2.5V
6:GND

P8
HEADER-SOCKET

P9
HEADER-SOCKET

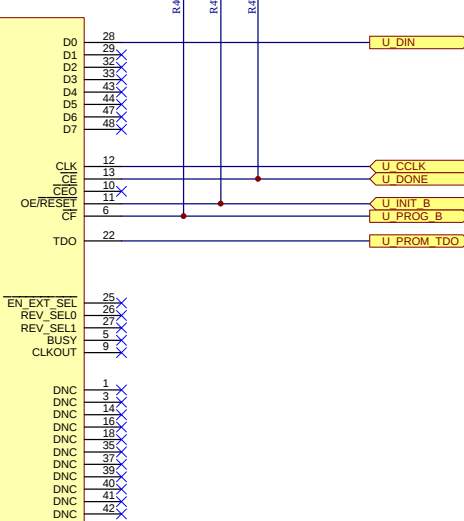
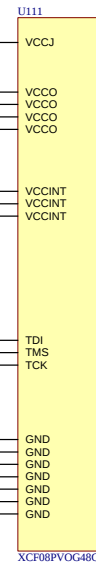
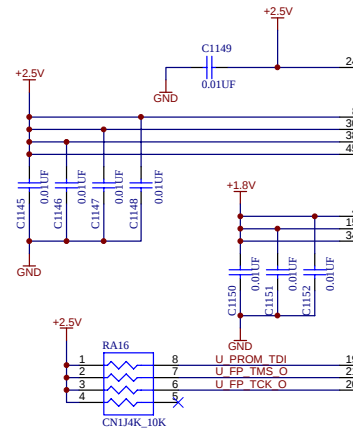
P10
HEADER-SOCKET

P11
HEADER-SOCKET

SILK

1:2:U_JTAG
2:3:S_FPGA

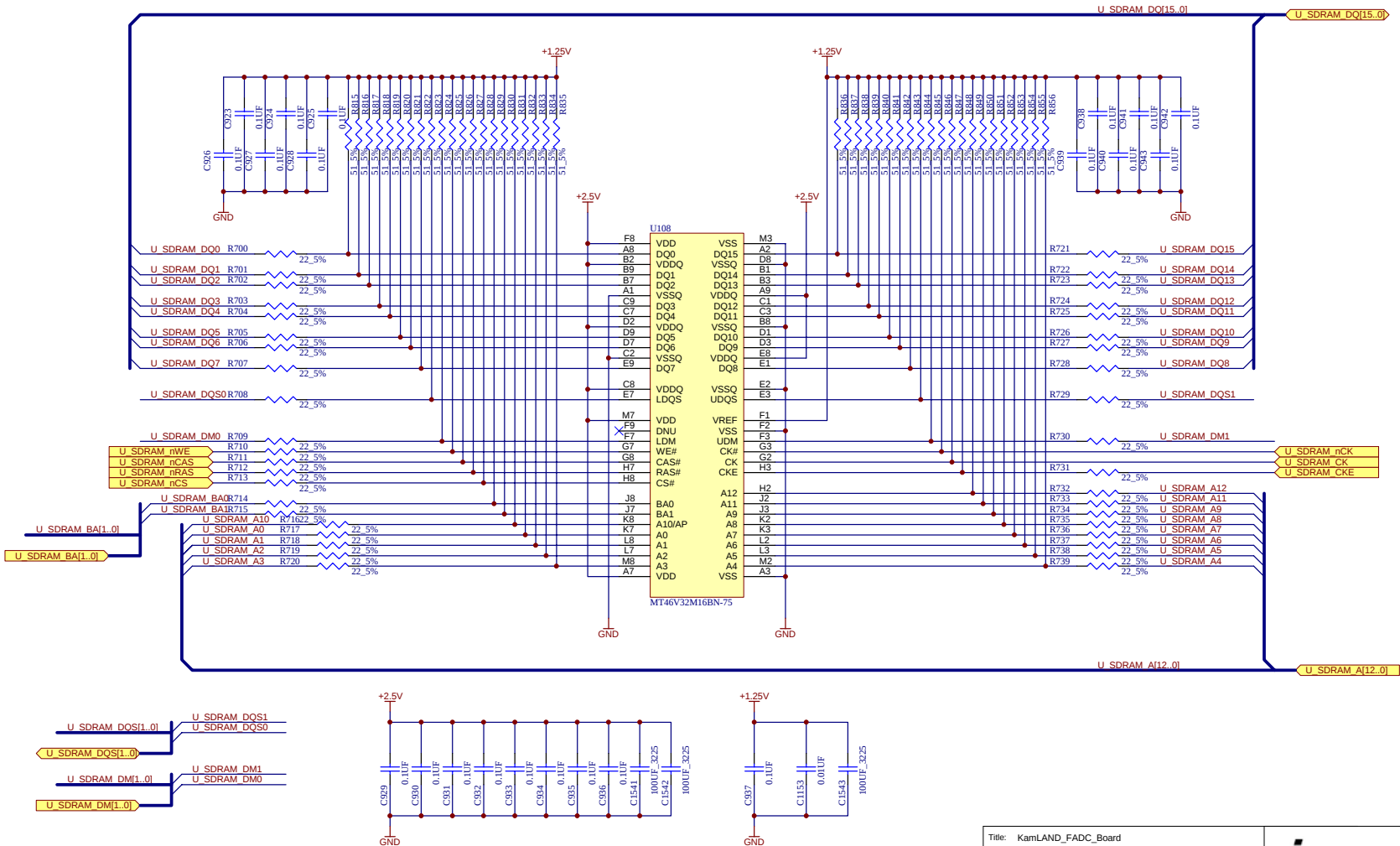
Default:2-3



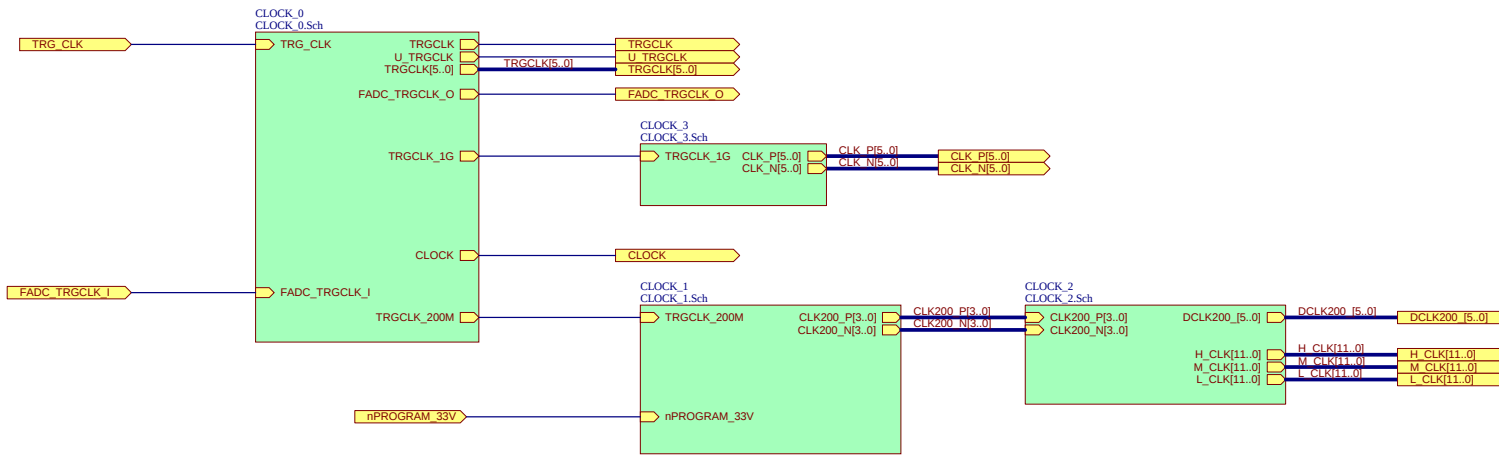
Title: KamLAND_FADC_Board		
Size: A3	Number: CCSC60002-2110	Revision: 2.00.00
Date: 27-Jul-2007	Time: 17:45:47	Sheet: 116 of 142
File: U_Config.Sch		

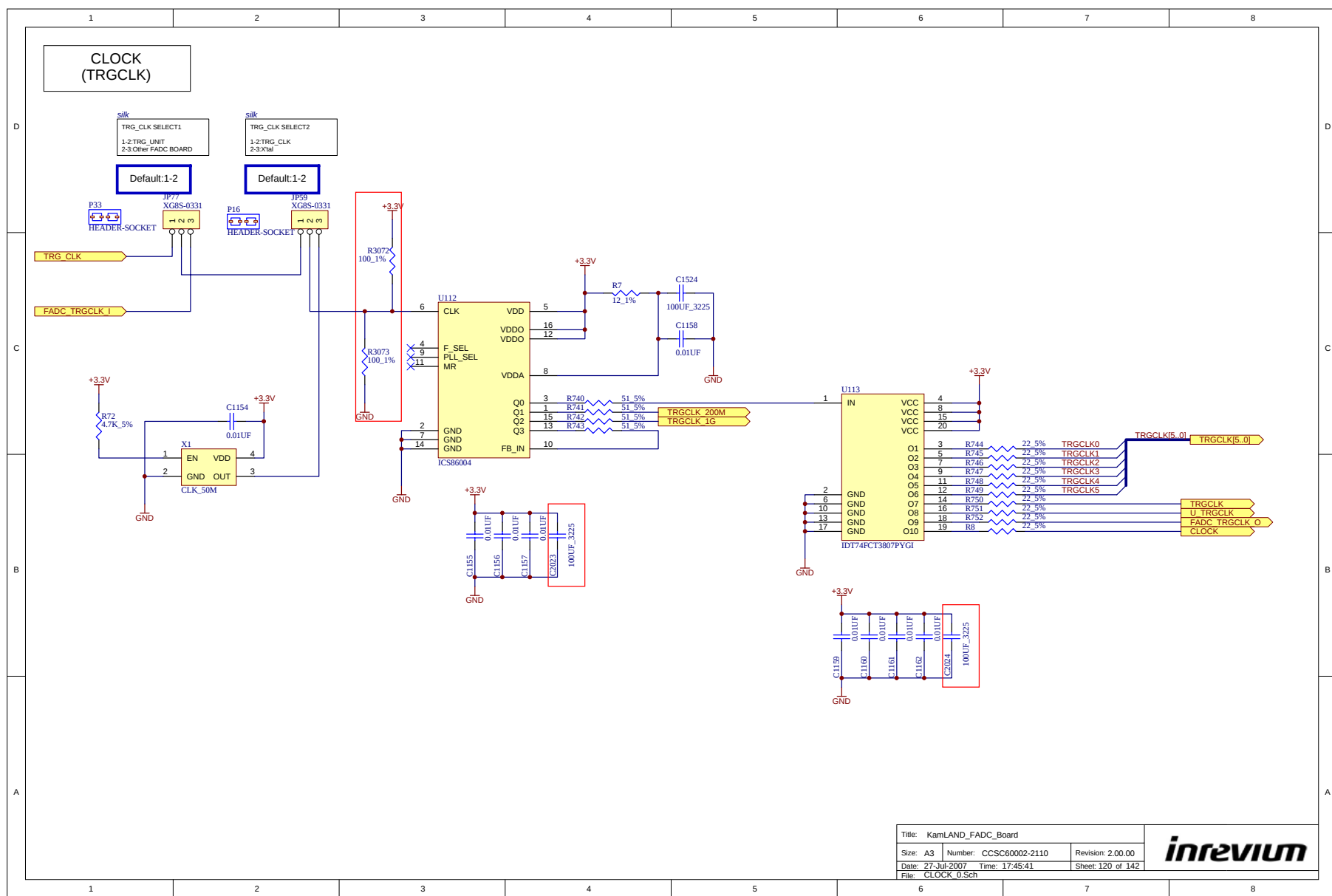
inrevium

DDR SDRAM (USER FPGA)

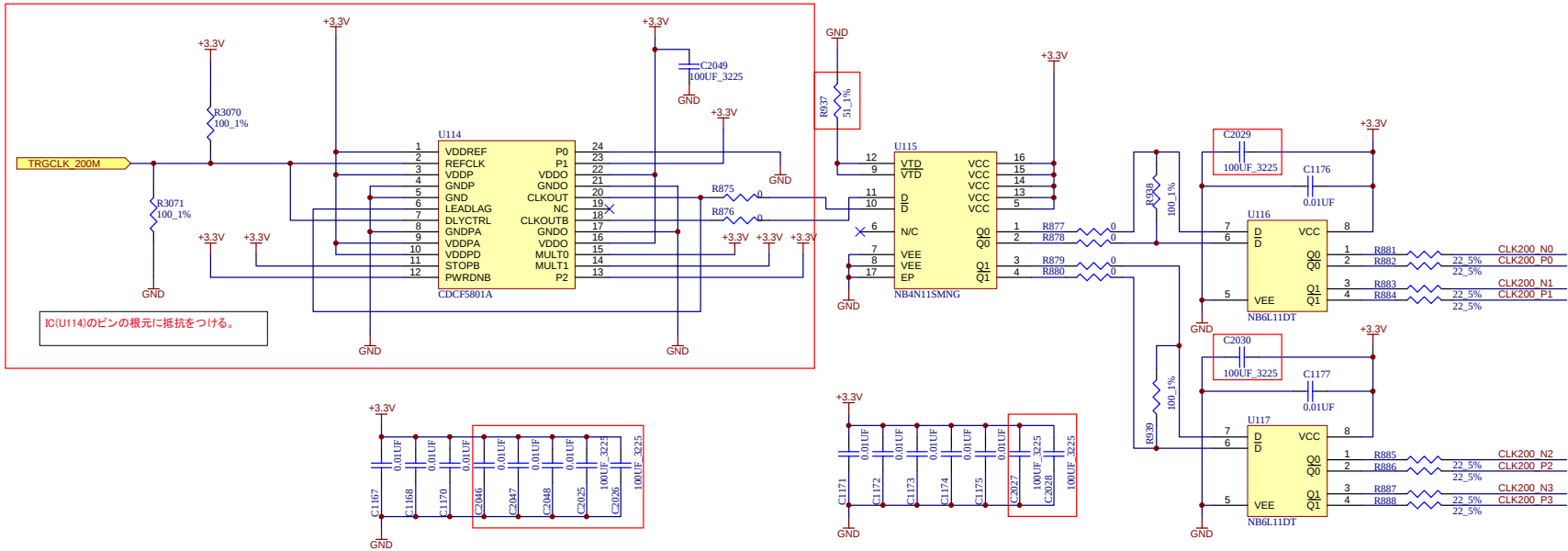


CLOCK TOP



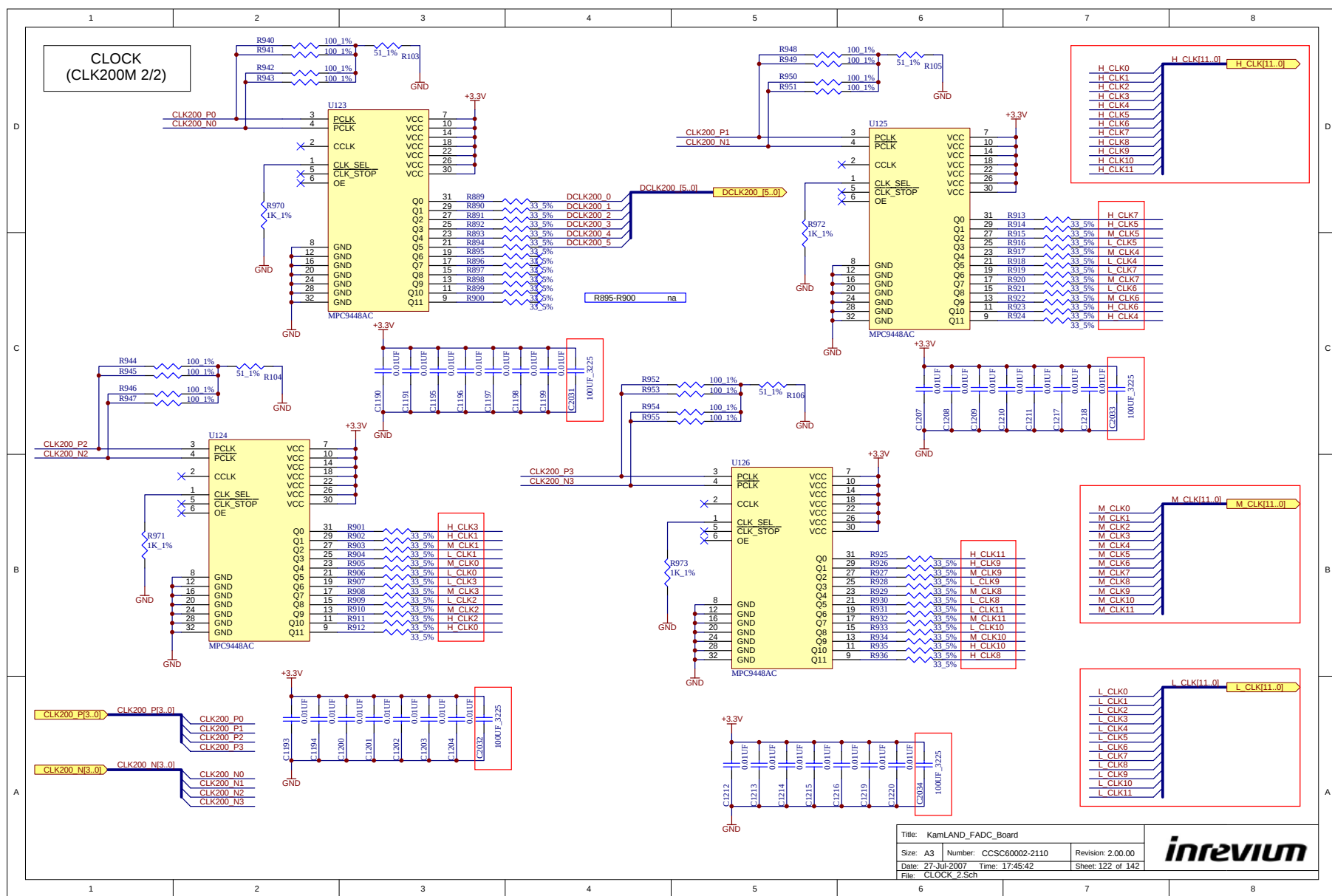


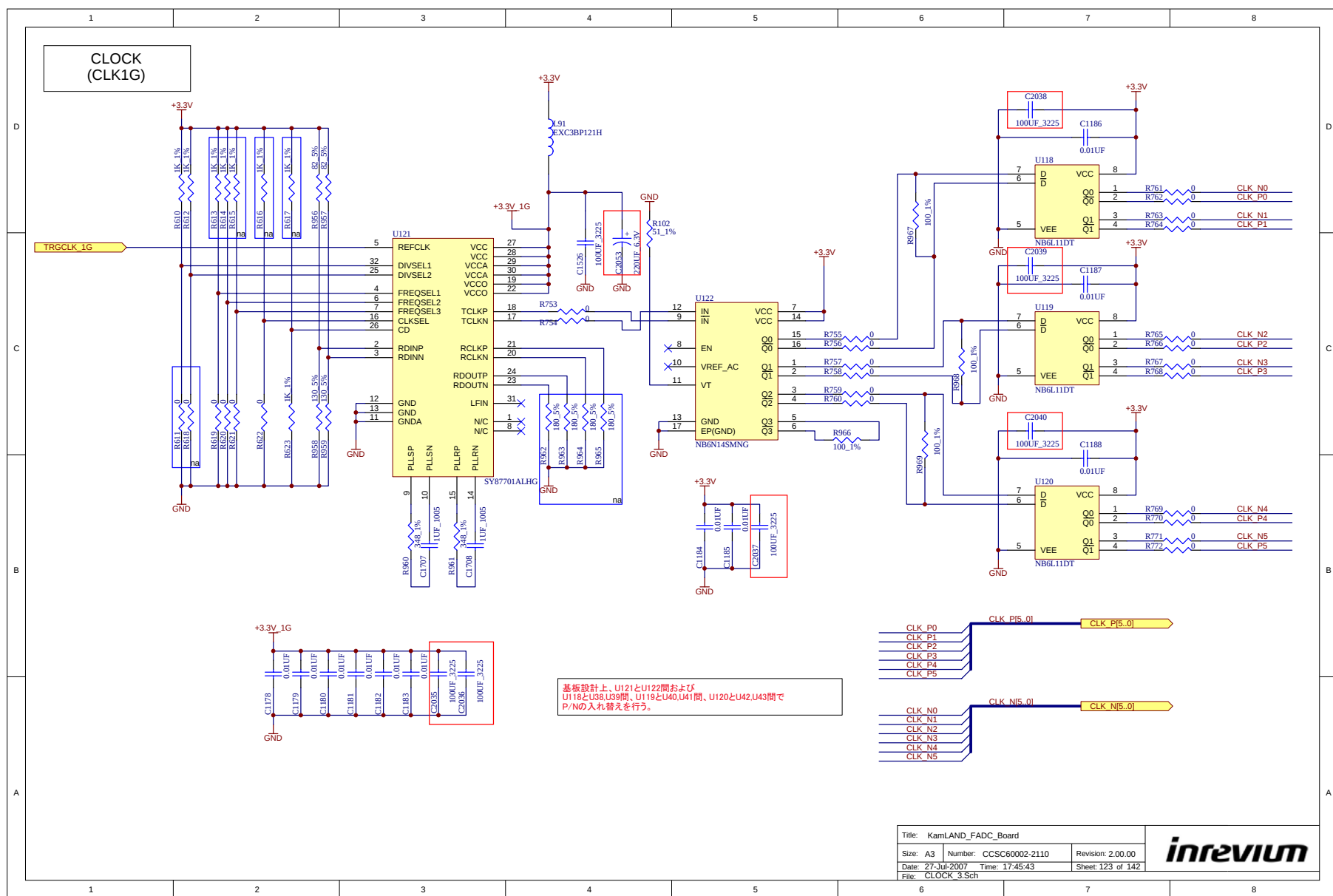
CLOCK (CLK200M 1/2)



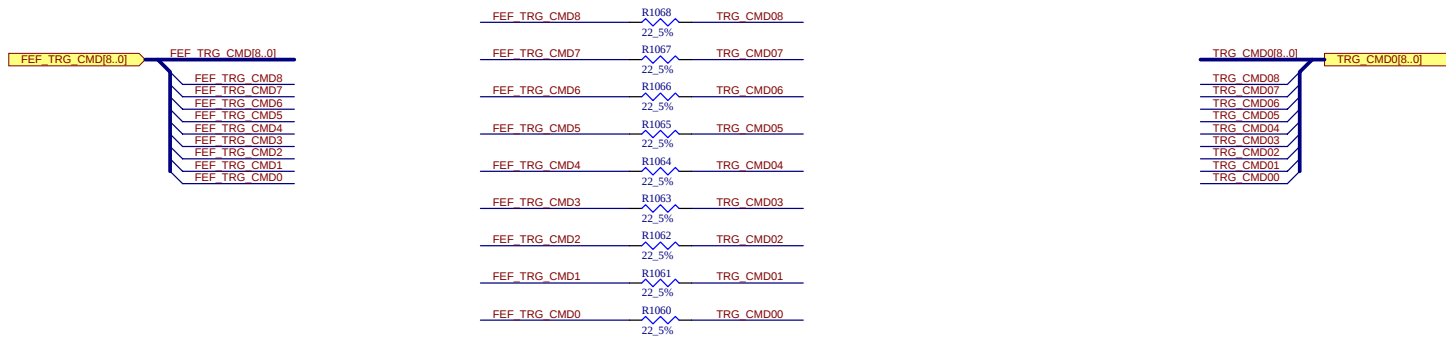
IC(U114)のピンの根元に抵抗をつける。

基板設計上、U114とU115間および
U116とU123間、U116とU125間、U117とU124間、U117とU126間で
P/Nの入れ替えを行う。



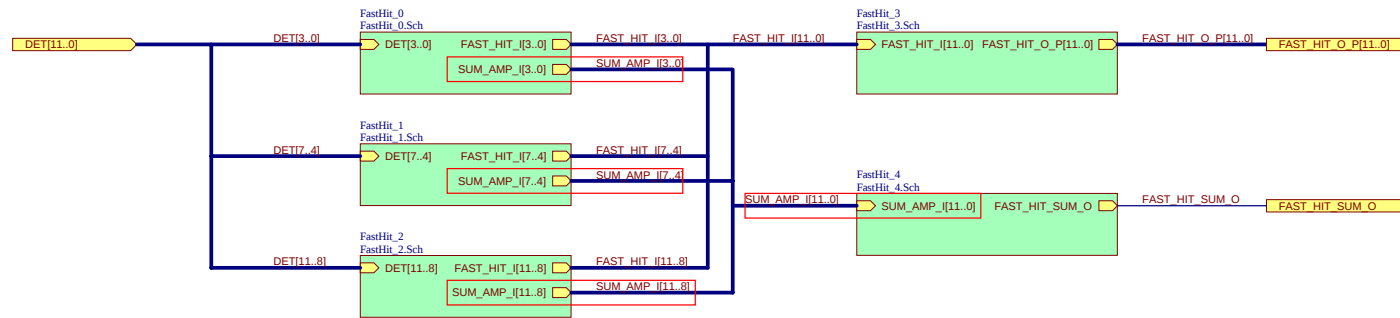


TRIGGER COMMAND DIVIDER

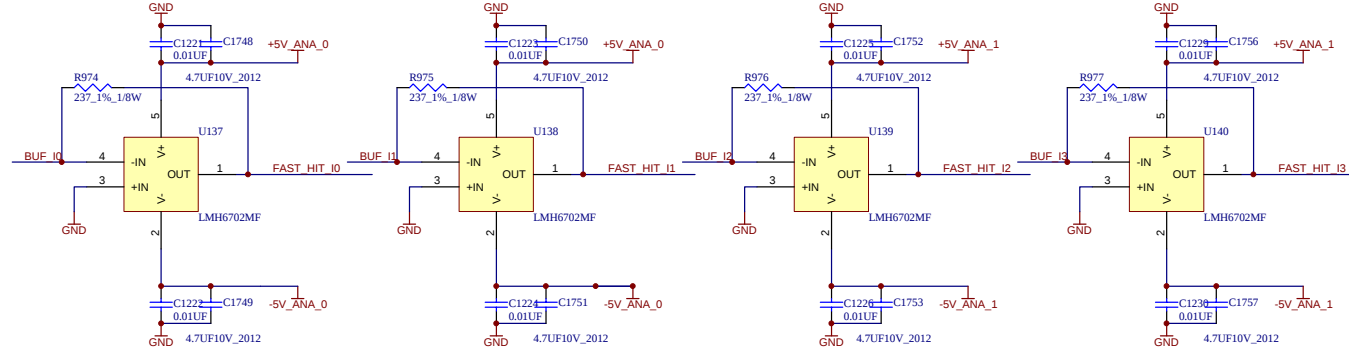
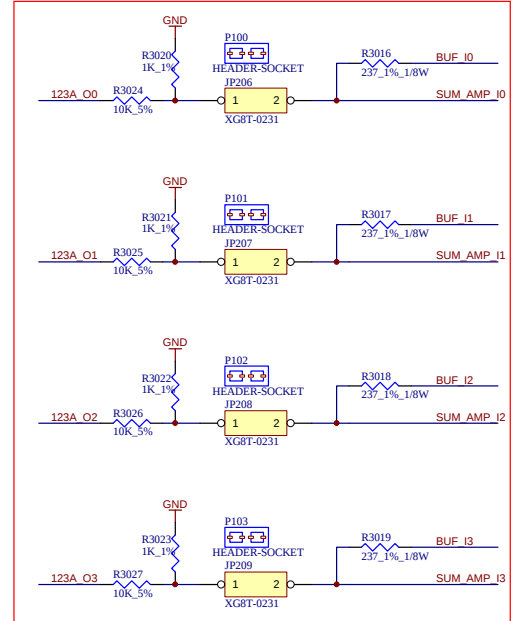
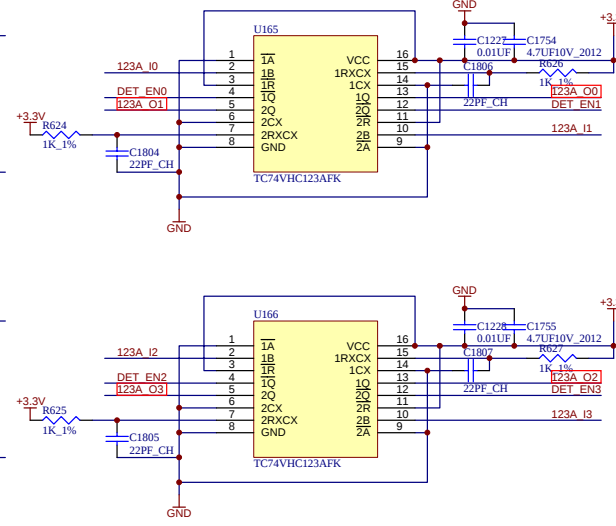
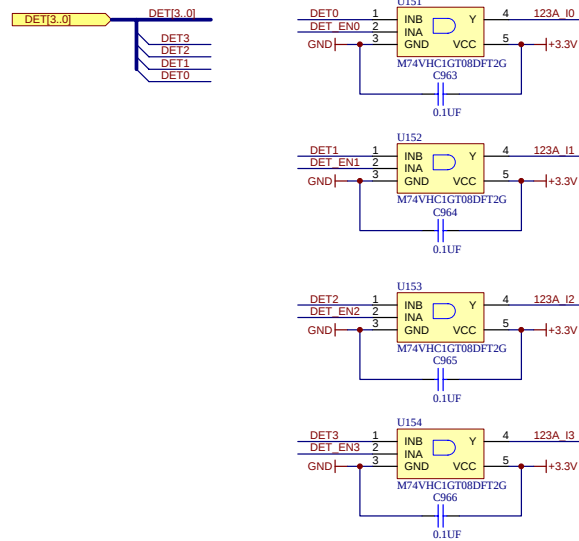


TRG_CMD00はR1060端からFEF0(U44)、FEF1(U45)、FEF2(U46)、FEF3(U47)、FEF4(U48)、FEF5(U49)に
反射を考慮した配線とすること。
TRG_CMD08.01も同様。
R1060～R1068はU106近くに配置すること。

FAST HIT TOP

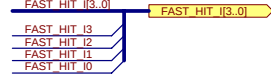
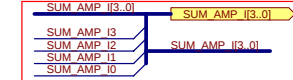


FAST HIT
DET[3..0] to FAST HIT

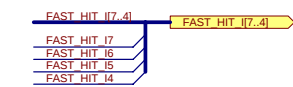
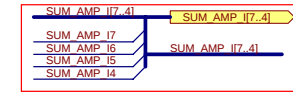
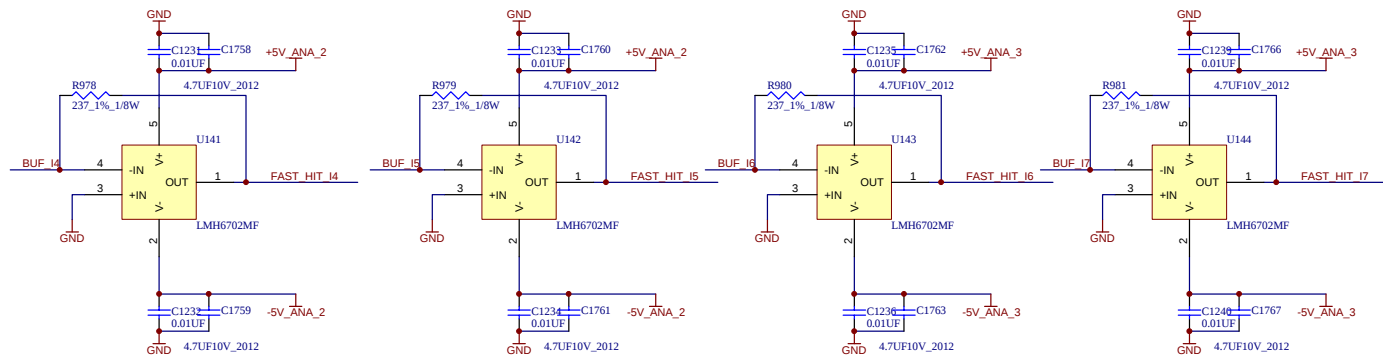
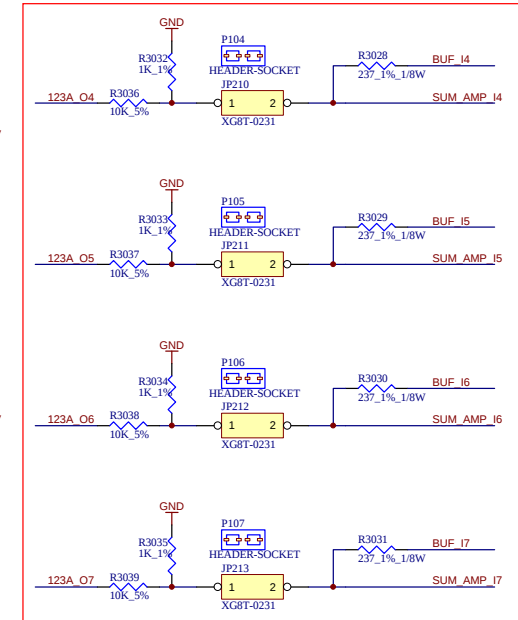
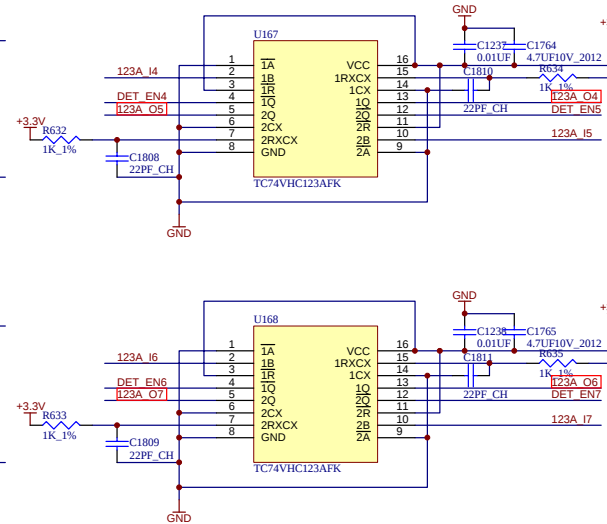
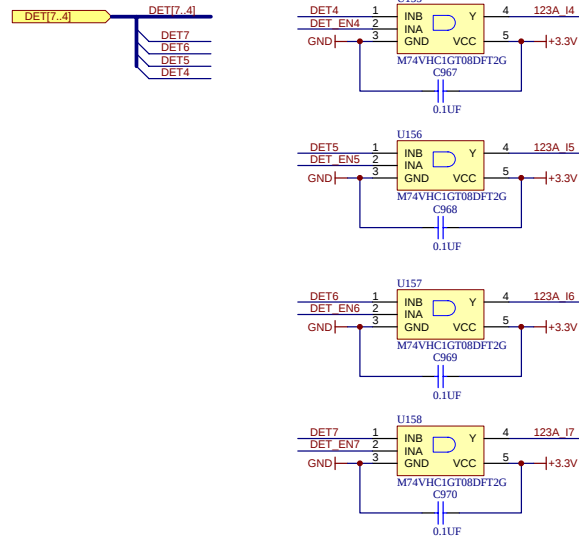


SILK FastHit select

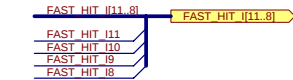
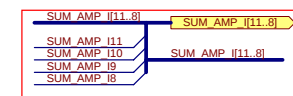
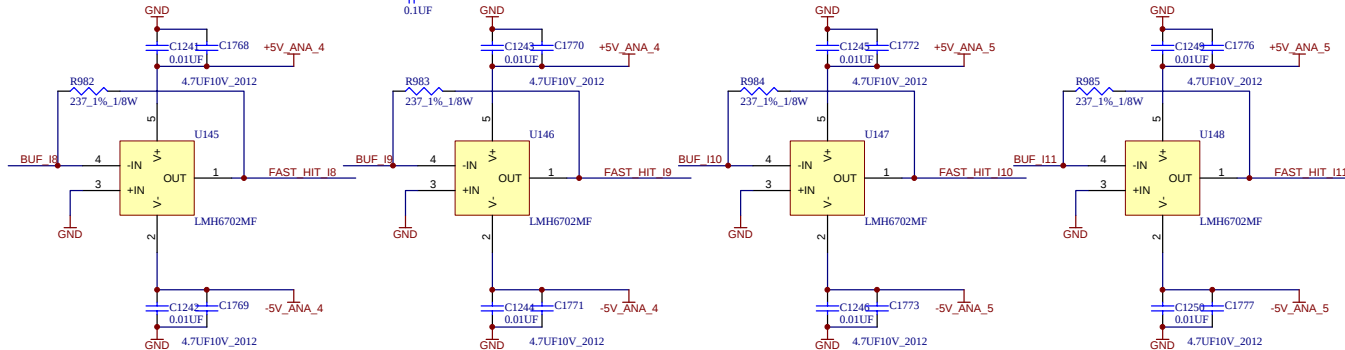
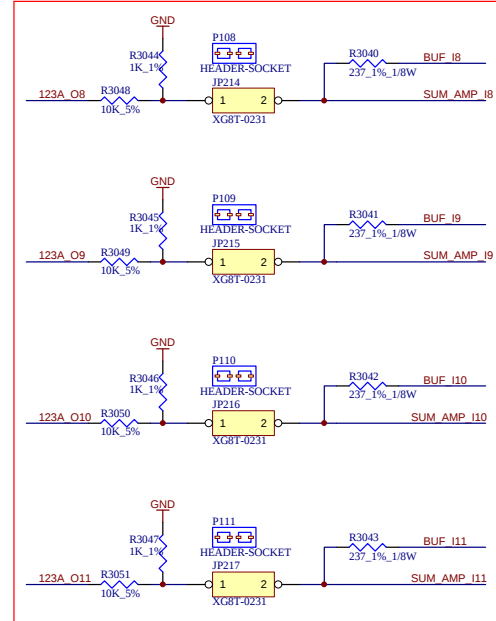
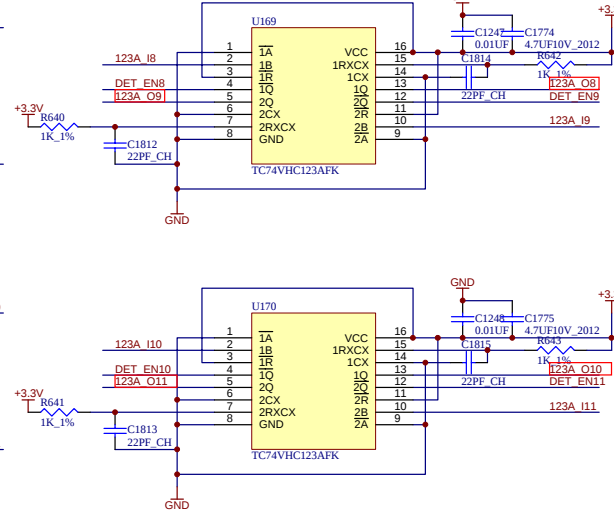
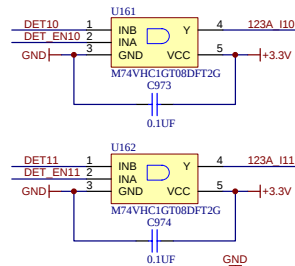
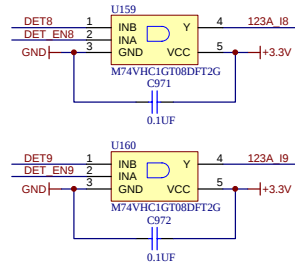
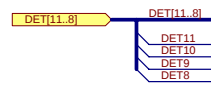
JP206-JP217を白線で囲む



FAST HIT
DET[7..4] to FAST HIT

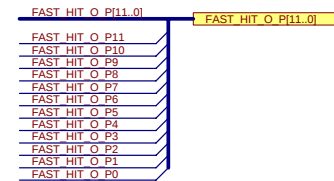
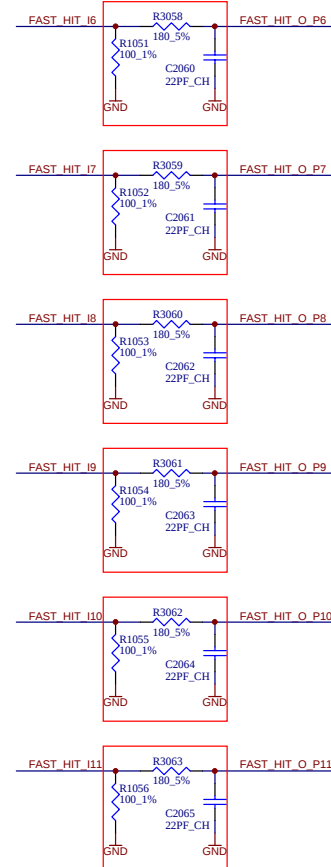
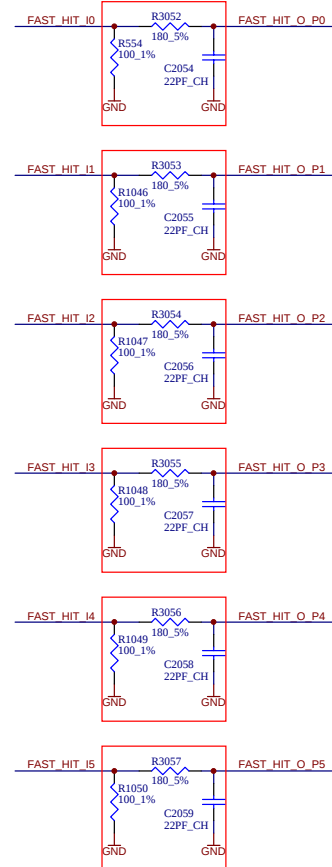
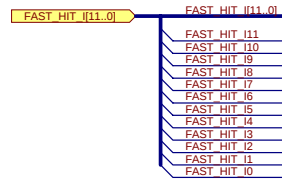


FAST HIT
DET[11..8] to FAST HIT



FAST HIT
FAST HIT OUT
(SingleEnd to Balance)

外部50Ω受時
50mV



Title: KamLAND_FADC_Board

Size: A3 Number: CCSC60002-2110 Revision: 2.00.00

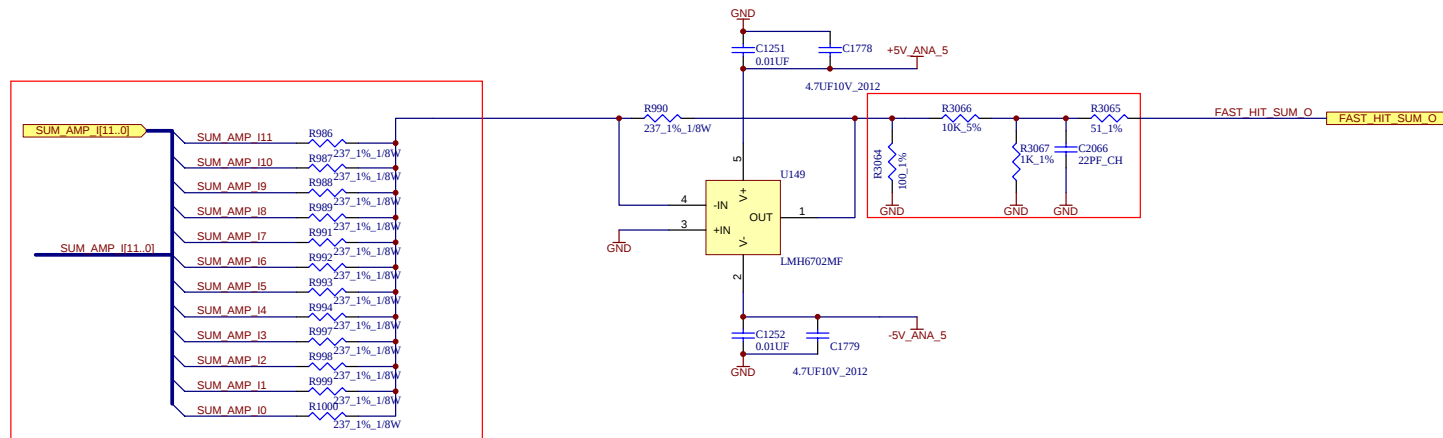
Date: 27-Jul-2007 Time: 17:45:30 Sheet: 129 of 142

File: FastHit_3.Sch

inrevium

FAST HIT
FAST HIT SUM

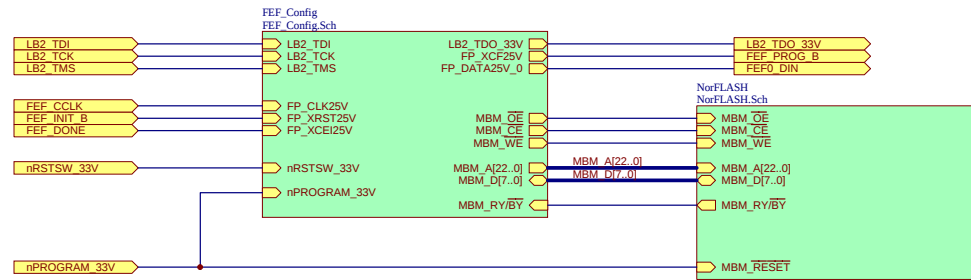
外部50Ω受時
10mV/ch



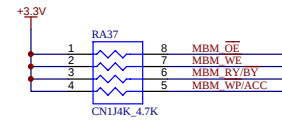
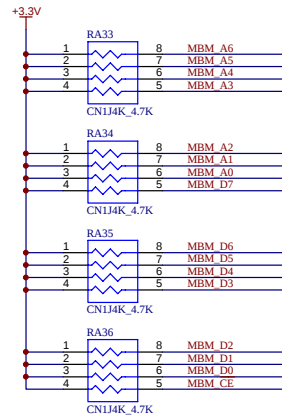
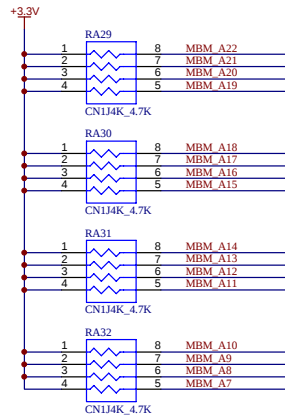
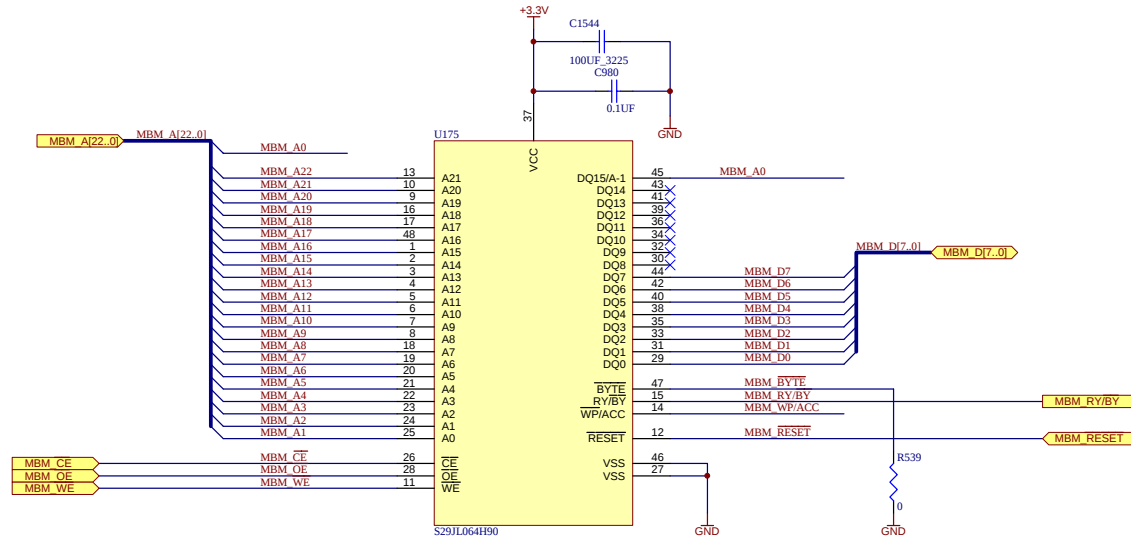
Title: KamLAND_FADC_Board		
Size: A3	Number: CCSC60002-2110	Revision: 2.00.00
Date: 27-Jul-2007	Time: 17:45:31	Sheet: 130 of 142
File: FastHit_4.Sch		

inrevium

FrontEnd FPGA CONFIG TOP

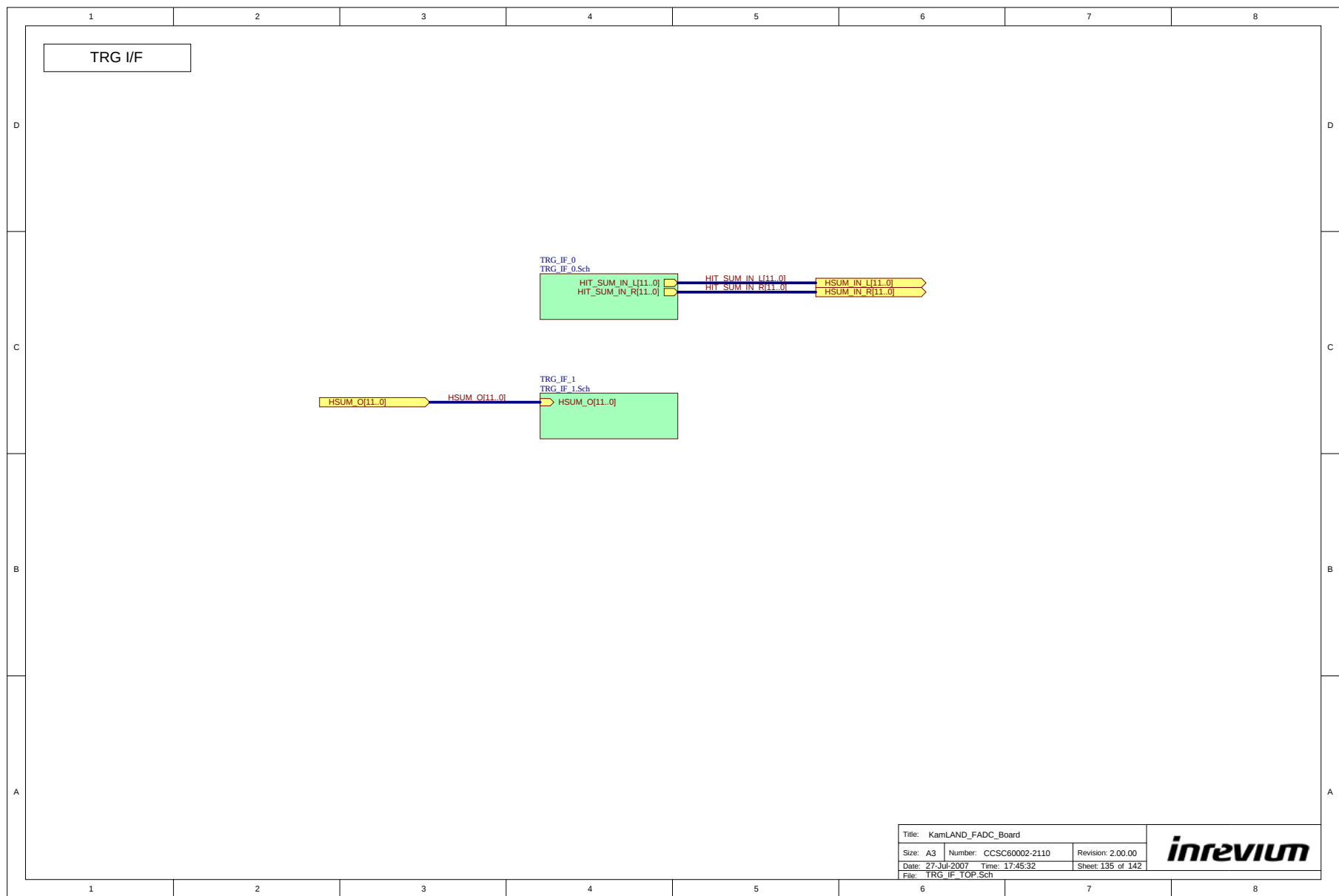


FLASH MEMORY



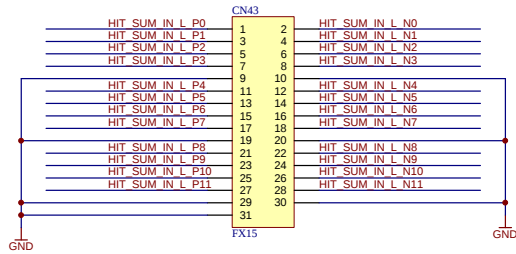
Title: KamLAND_FADC_Board		Revision: 2.00.00	
Size: A3	Number: CCSC60002-2110	Date: 27-Jul-2007	
Time: 17:45:49		Sheet: 134 of 142	
File: NorFLASH.Sch			

inrevium



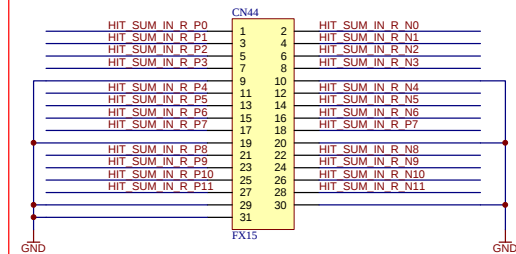
TRG I/F
HIT_SUM_IN(LVDS)

IN L

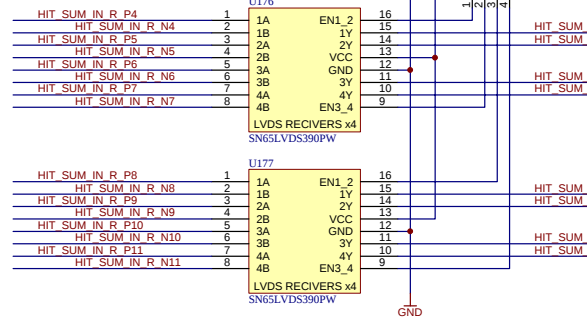
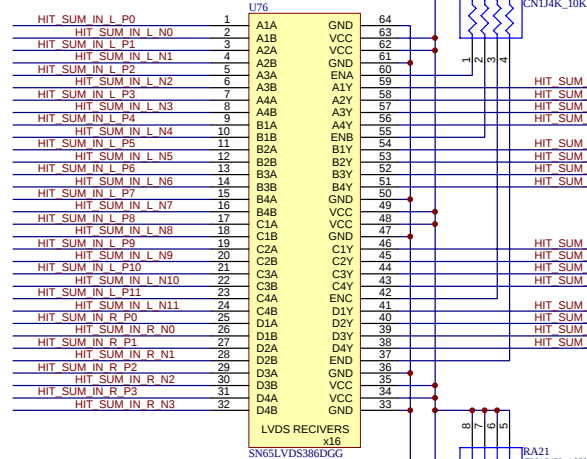
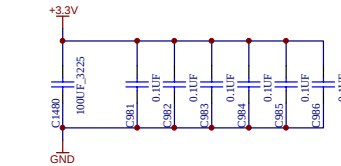


HIT_SUM_IN L P0	R389	100 5%	HIT_SUM_IN L N0
HIT_SUM_IN L P1	R390	100 5%	HIT_SUM_IN L N1
HIT_SUM_IN L P2	R391	100 5%	HIT_SUM_IN L N2
HIT_SUM_IN L P3	R392	100 5%	HIT_SUM_IN L N3
HIT_SUM_IN L P4	R393	100 5%	HIT_SUM_IN L N4
HIT_SUM_IN L P5	R394	100 5%	HIT_SUM_IN L N5
HIT_SUM_IN L P6	R395	100 5%	HIT_SUM_IN L N6
HIT_SUM_IN L P7	R396	100 5%	HIT_SUM_IN L N7
HIT_SUM_IN L P8	R397	100 5%	HIT_SUM_IN L N8
HIT_SUM_IN L P9	R398	100 5%	HIT_SUM_IN L N9
HIT_SUM_IN L P10	R399	100 5%	HIT_SUM_IN L N10
HIT_SUM_IN L P11	R400	100 5%	HIT_SUM_IN L N11

IN R



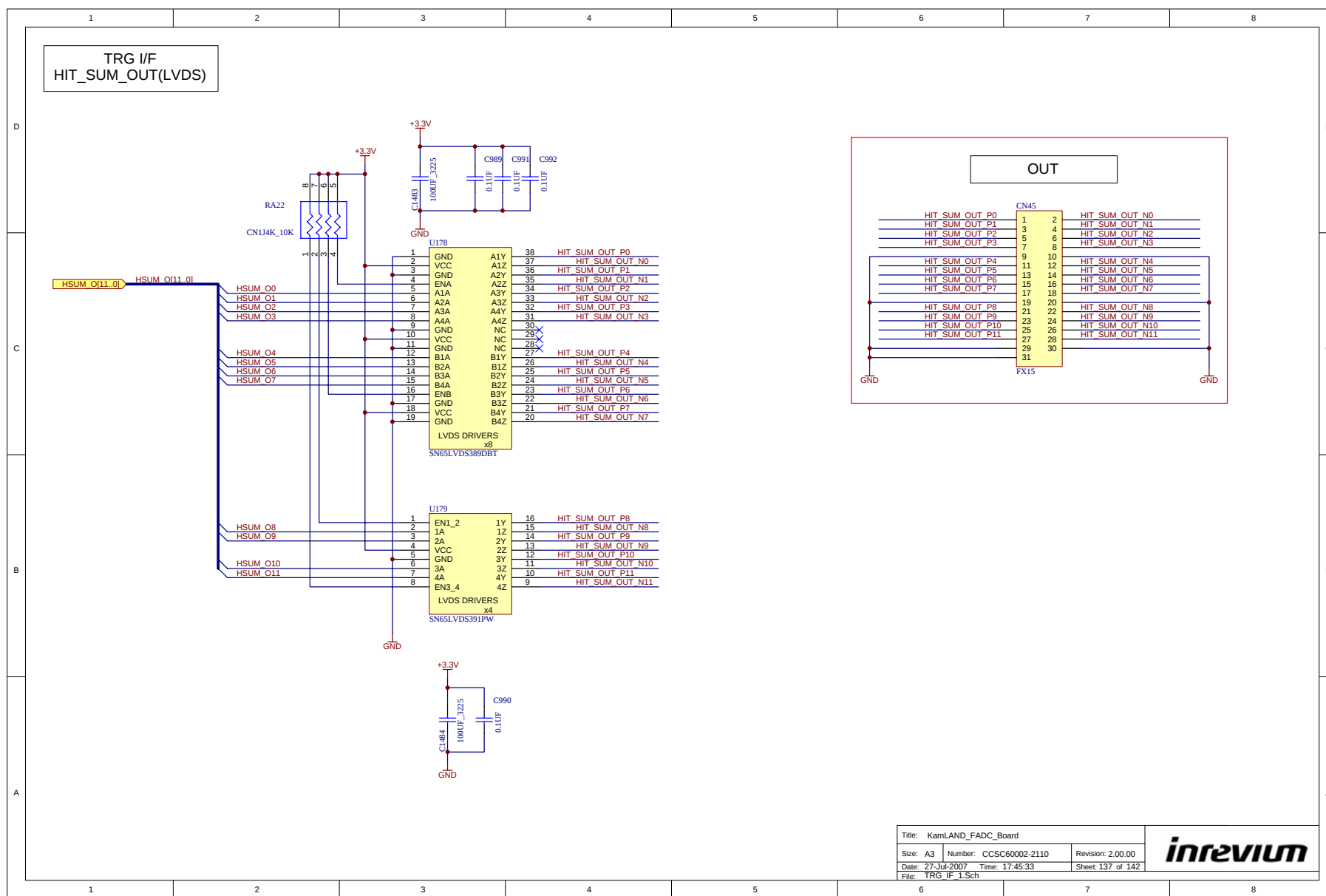
HIT_SUM_IN R P0	R401	100 5%	HIT_SUM_IN R N0
HIT_SUM_IN R P1	R402	100 5%	HIT_SUM_IN R N1
HIT_SUM_IN R P2	R403	100 5%	HIT_SUM_IN R N2
HIT_SUM_IN R P3	R404	100 5%	HIT_SUM_IN R N3
HIT_SUM_IN R P4	R405	100 5%	HIT_SUM_IN R N4
HIT_SUM_IN R P5	R406	100 5%	HIT_SUM_IN R N5
HIT_SUM_IN R P6	R407	100 5%	HIT_SUM_IN R N6
HIT_SUM_IN R P7	R408	100 5%	HIT_SUM_IN R N7
HIT_SUM_IN R P8	R409	100 5%	HIT_SUM_IN R N8
HIT_SUM_IN R P9	R410	100 5%	HIT_SUM_IN R N9
HIT_SUM_IN R P10	R411	100 5%	HIT_SUM_IN R N10
HIT_SUM_IN R P11	R412	100 5%	HIT_SUM_IN R N11

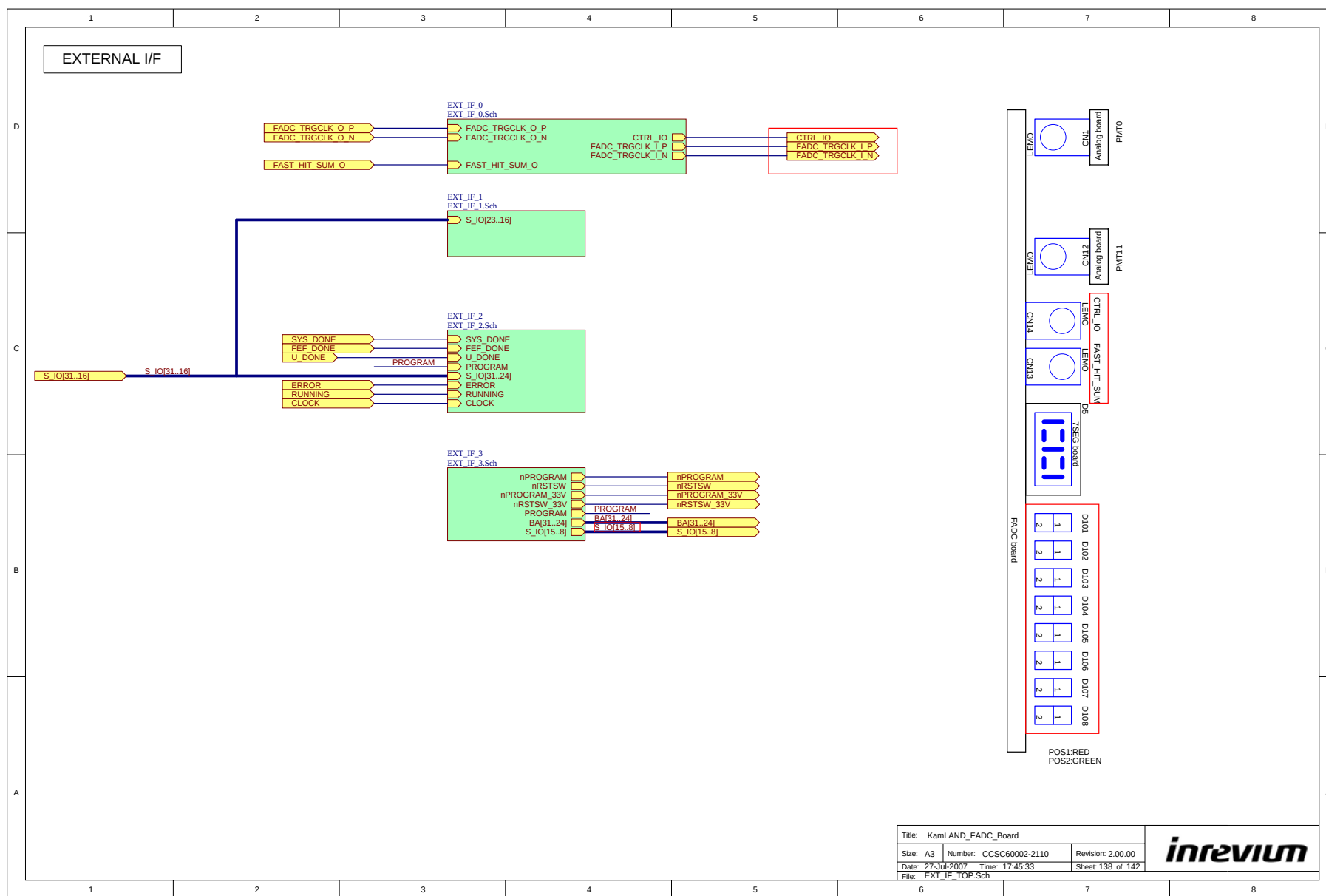


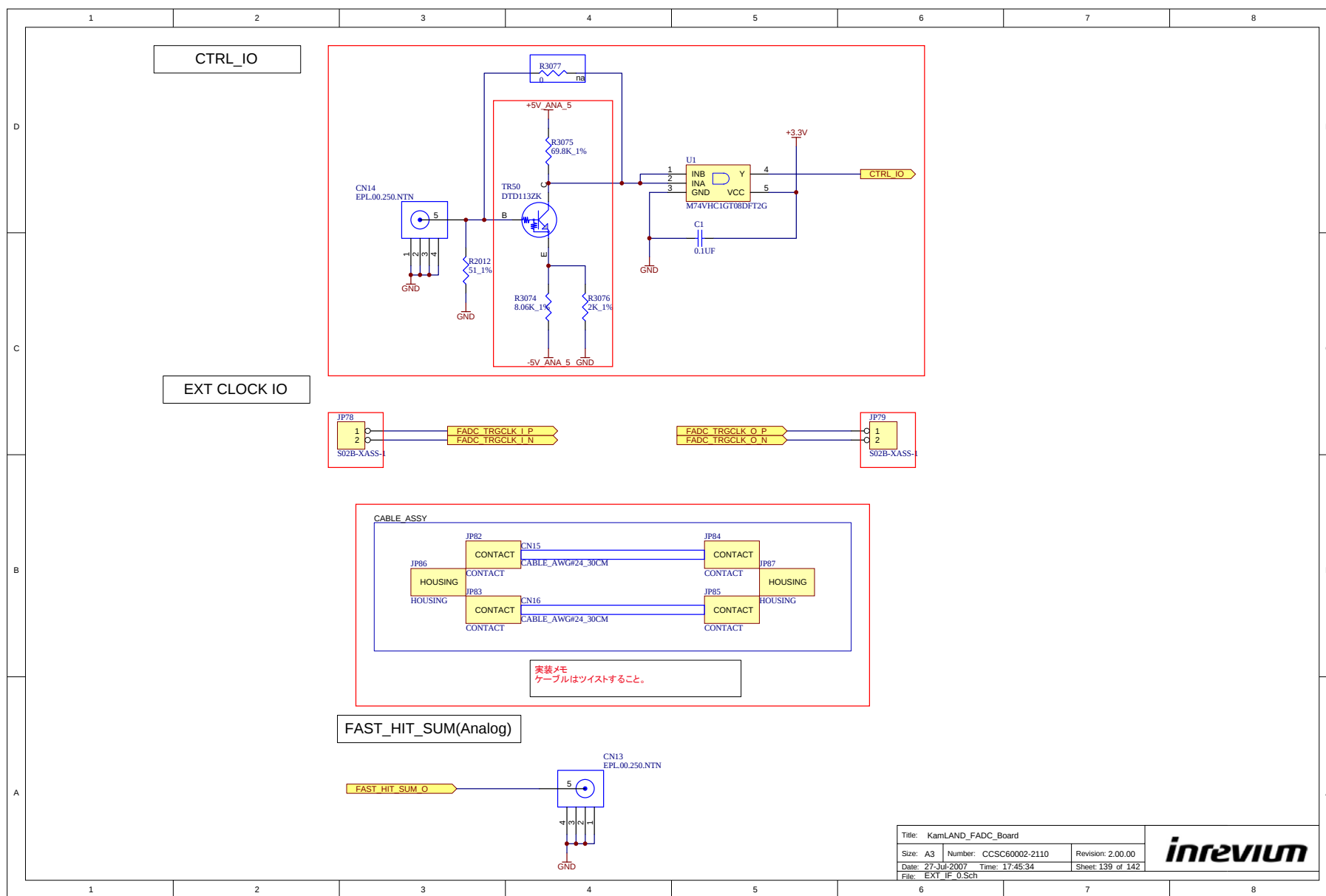
Title: KamLAND_FADC_Board

Size: A3 Number: CCSC60002-2110 Revision: 2.00.00
Date: 27-Jul-2007 Time: 17:45:32 Sheet: 136 of 142
File: TRG I/F 0.Sch

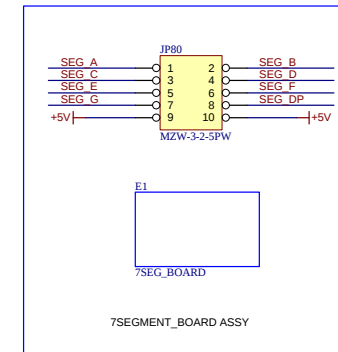
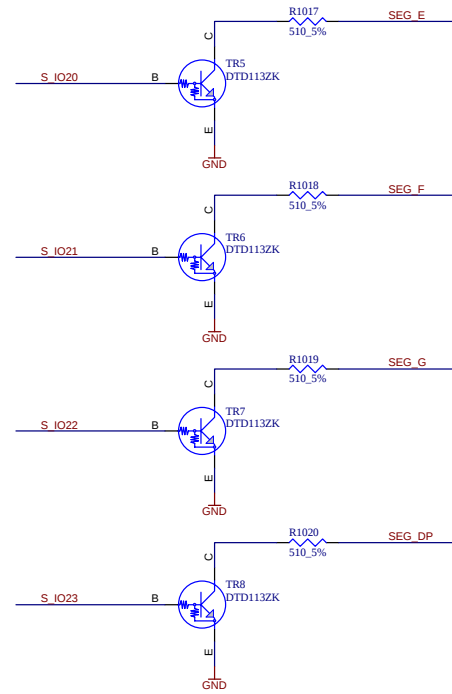
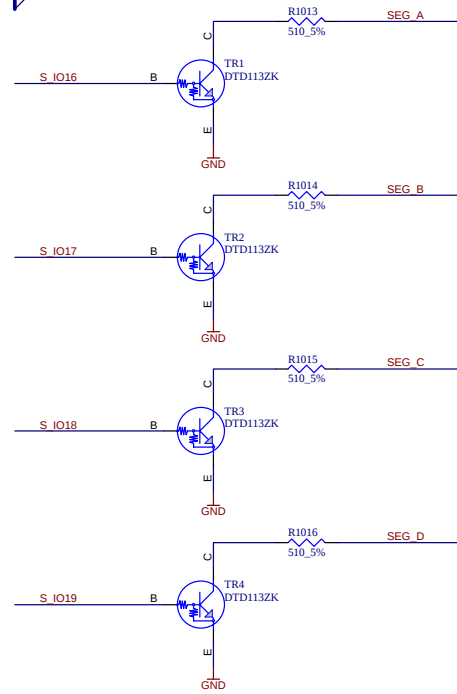
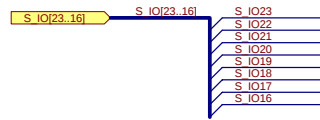
inrevium



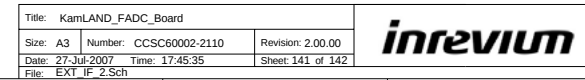




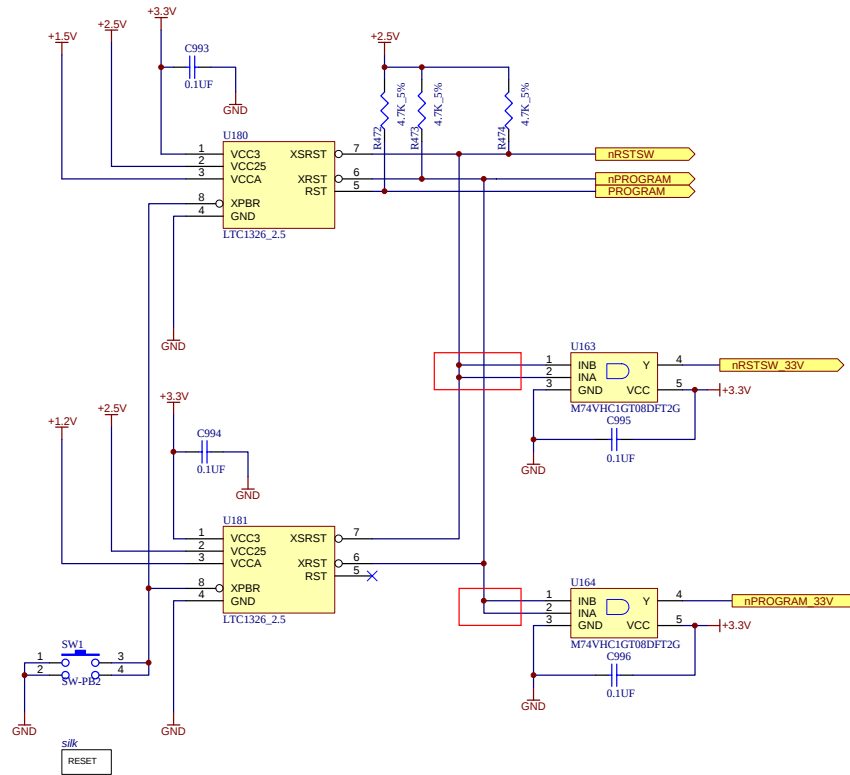
PANEL LED



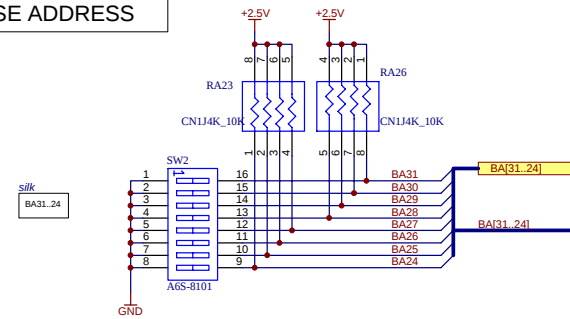
実装メモ
FADC基板に7SEG基板を接続する。



Reset SW



BASE ADDRESS



SYSTEM DEBUG

